Reduced-Wire Readout Systems-on-chip for High-Frequency Intravascular Ultrasound Imaging

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Reduced-Wire Readout Systems-on-chip for High-Frequency Intravascular Ultrasound Imaging

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SUMMARY

The objective of the proposed research is to minimize and integrate intravascular ultrasound imaging (IVUS) system on a guidewire. To achieve the object, wireless data communication for general capacitive micromachined ultrasonic transducer (CMUT) based ultrasound imaging system was proposed. Several innovative system- and circuit-level techniques are proposed towards the development of CMUT modeling, optimizing front-end circuits, wireless data communication, and inductive power transmission to reduce the system size and the required number of interconnections.

Since it provides real-time and high-resolution images of the arteries, intravascular ultra- sound (IVUS) has been a common imaging modality for cardio-vascular interventions. Current solid-state IVUS catheters (3F-8.2F in diameter) are bulky, cannot reach to lesions in narrow arteries, and require an additional catheter exchange, prolonging the critical cardio-vascular procedures. To address this issue, the way to integrate ASIC and CMUT array on a guidewire by reducing the number of connections is proposed in this research.

The proposed research presents three approaches to design and implement the reduced-wire IVUS system: 1) optimized the front-end circuit with properly modeled CMUT equivalent circuits, 2) on-chip quadrature sampler with time-division multiplexing (TDM) based on the synthetic aperture imaging algorithm, and 3) impulse-radio pulse width modulation (IR-PWM) for a wireless data acquisition.

The contributions of this research work are summarized as follows:

1. Development of an algorithm for optimization of a transimpedance amplifier (TIA) with lumped CMUT equivalent circuits.

2. Development of impulse radio pulse width modulation (IR-PWM) as a wireless data acquisition system. This work has been submitted to IEEE transactions on biomedical circuits and system.

3. Development of highly integrated transceiver for high-frequency CMUT array.

4. Development of wireless read-out system for CMUT-based IVUS system in chapter 4.
This work has been published in IEEE transactions on biomedical circuits and system ©2016.

CHAPTER 1. INTRODUCTION

Ultrasound has become outstanding imaging modality for diverse applications such as medical diagnosis and non-destructive inspection. From the discovery of piezoelectric effect by Pierre and Jacques Curie in 1880 [1], which enabled generation and perceiving of the high-frequency acoustic wave, research about the acoustics were accelerated, and the invention of the submarine detection by Paul Langevin during World war I ignited research on ultrasonics [2]. In the 1930s, people started research of interaction between human tissue and ultrasound, and a therapeutic usage of ultrasound, heating tissues, was the first achievement [3]. From the 1940s, researchers like John Julian Wild and John Reid intensely studied acoustic reflection from the soft tissue, and eventually, they developed a methodology of diagnostic medical ultrasound imaging. Siemens Medical Systems of Germany developed the methodology further and released Vidoson that is the first real-time ultrasound scanner. At the expense of many researchers' effort, medical ultrasound imaging has become mature, and people use its diverse applications. Intravascular imaging is one of the applications.

In the past four decades, angiography has been the most common detection methodology for cardiovascular diseases. In angiography, a surgeon makes a small hole in the blood vessel and passes a catheter through the hole into the vessel. The catheter works as a pipe which delivers contrast agents that absorb the x-rays. Once the contrast agents are injected, the vessel is distinguished from other tissues, and abnormally narrowed point of the vessel, where severe stenosis occurs, can be found [4]-[6]. As the previous sentence implies, the angiography can only diagnose severe stenosis which is already aggravated

too much to be treated without surgery. Because the basis of ultrasound imaging is an acoustic reflection from a different medium, intravascular ultrasound imaging (IVUS) can show the shape of the vessel. Stenosis is started from atherosclerosis that is buildup process of plaque, which piles up on the arterial wall and narrows the vessel. Compare to the vessel, the plaque is stiff material, so plaque can be distinguished from tissue in the IVUS image. It means IVUS can detect early stage of stenosis which can be cured with a minimal treatment [7]-[9]. In addition, when it compares to the angiography that only shows the 2-D silhouette of the vessel, the IVUS imaging can show a more detailed cross-sectional image of it. Over the past several decades, researchers have been studying side effects of the X-ray imaging and the fact that the X-ray imaging that is used on the angiography increases risk of cancer and genetic damages was proven [10]-[11]. Thus, the IVUS is the most promising modality to make up the shortcoming of the angiography that uses the X-ray for imaging.

1.1 Intravascular Ultrasound (IVUS) Imaging

Every year, tens of millions of people die of cardiovascular disease, the most cause of mortality among both men and women in the western World [12]. Therefore, the need for a diagnostic tool for heart arteries has substantially increased, leading to a lot of research on non-invasive cardiovascular imaging. Since it provides real-time detailed images of the arteries with low cost, ultrasound imaging is the most feasible imaging modality. Accordingly, intravascular ultrasound (IVUS) imaging, shown in Fig. 1.1, is introduced as a viable method of artery imaging for diagnosis and treatment of coronary artery diseases [13].

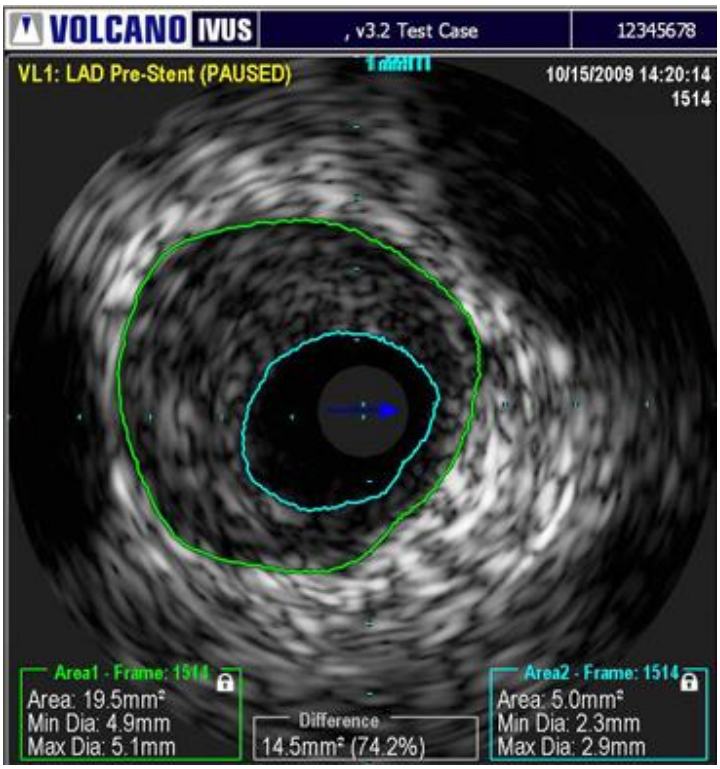
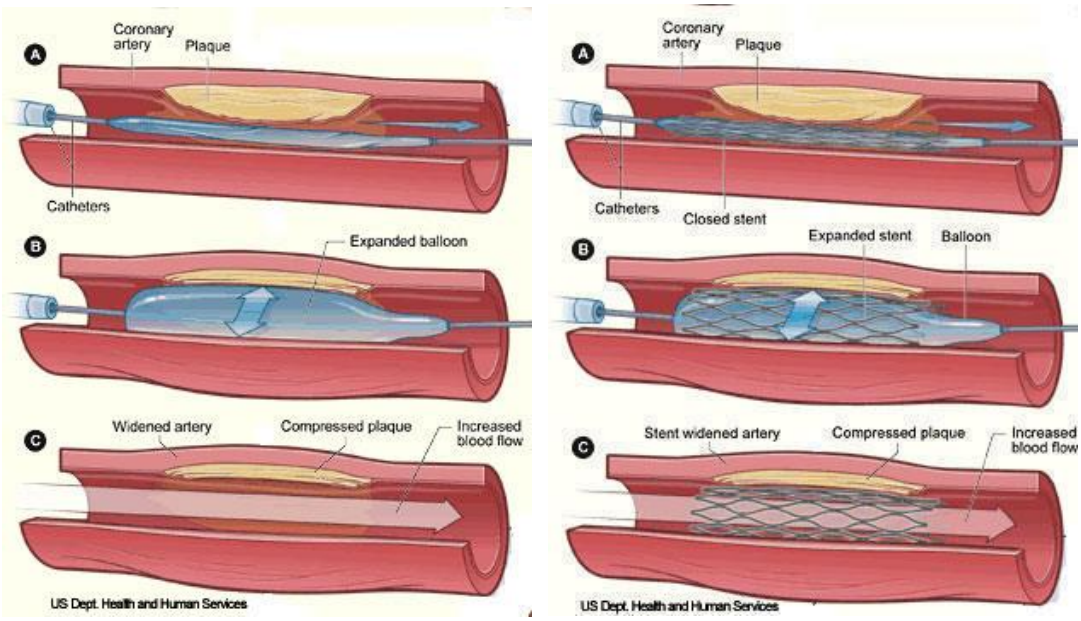


Figure 1.1. Exemplar IVUS image. Image courtesy of Volcano.

In IVUS imaging, a long and thin catheter is threaded into the heart of the patient through an artery [14], [15]. There are the various size of catheters, but the catheter of 2.5 to 5 French (0.87 to 1.43 mm) diameter [16] is generally used in the IVUS applications. At the tip of the catheter, a transducer which generates and receives ultrasound waves is placed. Because the diameter of the coronary artery is around 3.1 mm [17], the catheter and the transducer should be small enough to travel the lumen. On the other hand, because the artery is narrow and thin, the penetration depth of the IVUS imaging does not need to be far, and that allows increasing the operation frequency. Since lateral and axial resolutions are related to the operating frequency and the bandwidth of the transducer respectively, a high operating frequency (20 ~ 40 MHz) is preferable to balance the resolutions and penetration depth [18]-[21].



(a) (b)

Figure 1.2. (a) A pictorial diagram of the angioplasty procedure and (b) the stent placement procedure (adapted from [24]).

Currently, three different types of the IVUS catheters are commonly used: single element, multi-element array, and forward-looking catheter. The single-element catheter that has a transducer attached on certain direction can be relatively simple to design and minimized, but it requires mechanical rotation of the whole catheter [22]. On the other hand, the multi-element array catheter consists of multiple transducers, and they cover all directions to eliminate the requirement of rotation. Because the multiple elements should be connected to be controlled together, design complexity and size of the catheter are increased. Regarding the forward-looking catheter, transducers are placed at the tip of the catheter and headed for the front to see moving direction of the catheter not the side of the vessel wall [23].

There are two different general usages of the IVUS: a guide for percutaneous coronary intervention (PCI) and detection of plaques. All the treatments which are

performed to broaden the lumen of narrowed arteries including balloon angioplasty and stent placement are called PCI. Once a tiny balloon is inflated at the narrowed artery and pushes the plaque deposits on the wall of the artery, a stent is installed at the place to keep the artery open after the balloon is deflated (Fig. 1.2) [24]. Because the treatment should be on the exact point where stenosis occurs, visualization of the artery before, during, and after the intervention is required [25]. As mentioned previously, the IVUS is a valuable methodology for detection of early stage stenosis. A study about the IVUS (Providing Regional Observations to Study Predictors of Events in the Coronary Tree – PROSPECT) proved that the IVUS is a better modality for diagnosis of future heart diseases [26]. In addition, it is also important to distinguish volatile plaques that have a small fissure. The volatile plaque is easily ruptured, and the rupture causes clotting of a vessel, which is known as coronary artery thrombosis [24]. To distinguish the volatile plaque from the normal plaque, a silhouette of the artery is not enough, and detailed cross-sectional view of the artery is required.

The market of the IVUS is still expanding, and around 200,000 patients have taken the IVUS procedures in U.S. annually [14]. Although there is no reimbursement of the IVUS procedures in U.S, about 14% of PCI procedures used the IVUS. In Japan where the IVUS is reimbursed, around 65% of patients used the IVUS for a PCI procedure. It means the IVUS has a strong potential for growth, and limitation of angiography alone has been widely accepted.

1.2 Capacitive Micromachined Ultrasound Transducer (CMUT)

Currently, most of the medical ultrasound imaging utilizes piezoelectric transducer. However, in high-frequency applications that require minimum dimension and small

element spacing including the IVUS, it is hard to use piezoelectric transducers that have a limitation on small size element fabrication. In addition, the IVUS that needs to be inserted and navigate the vascular system requires a flexible tip of the catheter which carries transducer and associated electronics. Because of this consideration, the size of the tip should be small enough, and transducer and electronics should have short width and length. Thus, integration of transducer and electronics are highly desired to reduce dimension and interconnections, but, because of fabrication characteristics of a piezoelectric transducer, it is not easy to be integrated with CMOS. From the needs for addressing those limitations, a capacitive micromachined ultrasound transducer (CMUT) was introduced [27]-[30].

The basic concept of CMUTs was announced in the same age of early piezoelectric transducers [31]. However, the CMUT's requirement of strong electric field strength (10^6-V/cm), which was hard to be achieved with the silicon technology of the time, impeded wide usage of CMUTs. As time goes on, semiconductor fabrication technology has been rapidly advanced, and the strong electric field strength has become a viable option. CMUTs have several advantages against to the piezoelectric transducer: low-cost, ease of large array fabrication, and integration with electronics. All the merits are coming from the nature of CMUT fabrication methodology that is processed by following steps. First, a silicon wafer is heavily doped to work as a bottom electrode of the transducer. Then, silicon nitride that is a dielectric material is deposited on the doped silicon as a protective insulator. Amorphous silicon is deposited on the insulator, patterned by photolithography, and etched to make a sacrificial layer for the vacuum gap. Silicon nitride is deposited over the surface, and narrow through-holes are etched to make a passage for the etchant to access the sacrificial layer. After the etchant removes all the sacrificial layer, the membrane is

released, a silicon nitride is deposited again to block the holes. Then, Aluminum top electrodes are placed above the sacrificial layer by metallization, and a low-temperature-oxide is deposited as a passivation layer [32], [33]. All the steps are the same as the semiconductor technology that is already matured to fabricate dense small arrays with sufficient yield and reduced cost. In addition, because the CMUT fabrication steps do not require high-temperature process and can be fabricated with integrated circuit (IC), the CMUT can be easily fabricated on the electronics without external interconnections [34].

Dimension-limited applications like the IVUS, interconnection between CMUT and electronics is one of the most important factors. Direct connection between CMUT and IC reduces dimension and parasitic capacitance which reduces the SNR slightly. There are several approaches for the integration of CMUT and CMOS: CMUT-in-CMOS, interleaved CMUT-CMOS, Flip chip bonding, and CMUT-on-CMOS. CMUT-in-CMOS approach simultaneously process CMUTs with CMOS [35]. This parallel processing reduces cost and time, but, because the CMUT fabrication has to follow CMOS fabrication properties, the CMUT processes is limited in terms of material type and layer thickness, which limits the performance of the CMUT. Moreover, as the CMUT should be next to the CMOS not under the CMOS, the area is increased. There is another approach which called interleaved CMUT-CMOS. In this method, interrupt IC fabrication during deposition of thin gap height, which improves the performance of the CMUT [36], [37]. In this method, design complexity increased compare to the CMUT-in-CMOS, and the CMOS should still be placed next to the CMUT, which increases area. To integrate CMUT and CMOS without increasing area and degrading performance of CMUT, separately fabricated the CMUT and CMOS are connected through flip chip bonding [38]-[43]. In this case, both of the CMUT

and CMOS can get the best performance, but flip-chip bonding requires some additional fabrication steps and complex packaging technique [44]. Furthermore, the solder bump limits the minimum size of the CMUT array [45]. To address those limitations, CMUT-on-CMOS, which fabricates the CMUT directly on the fabricated the CMOS, was introduced [46], [47]. To avoid damaging the CMOS during the CMUT fabrication, high-temperature processes are prohibited in the CMUT-on-CMOS that improves the quality of isolation layer [48].

1.3 Principle of ultrasound imaging

Fundamental of the ultrasound imaging is measuring elasticity and density of the imaging target. In medical ultrasound, since the tissue and blood mostly consist of the water, longitudinal waves are propagated, and the velocity of it is

$$c = \sqrt{\frac{K}{\rho}}, \tag{1.1}$$

where ρ is the density and K is incompressibility of the bulk modulus [49]. The average acoustic wave velocity is 1540 m/s for the soft tissue. Accordingly, the wavelength of acoustic wave is

$$\lambda = \frac{c}{f}, \tag{1.2}$$

where f is the operating frequency.

Most of the ultrasound imaging use reflection mode, which is also referred as pulse-echo imaging. In this mode, first, a transmitter applies an electrical pulse to a transducer, which converts the electrical signal to acoustic wave and vice versa, the

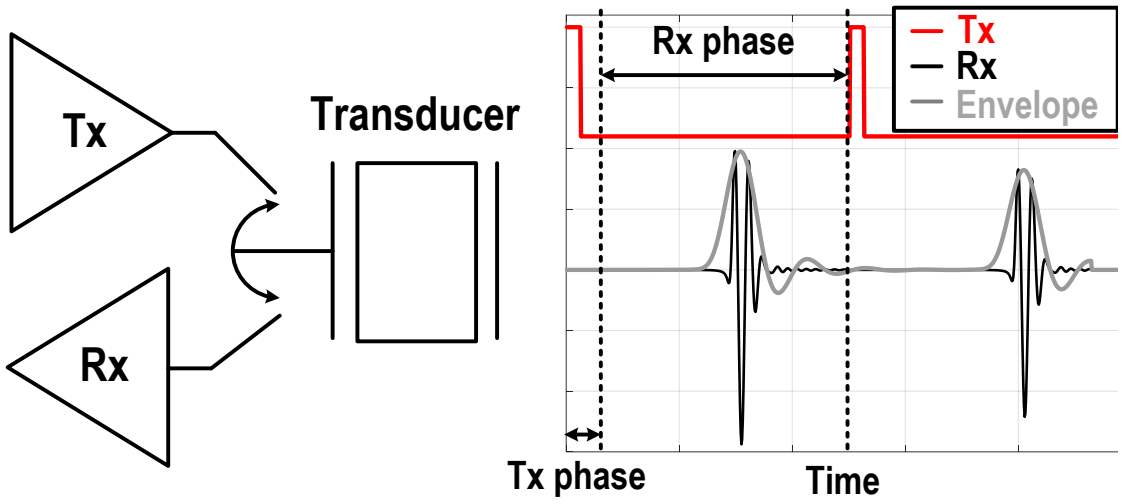


Figure 1. 3. Illustration of pulse-echo operation for A-scan. At the transmitter (Tx) phase, the transducer converts electrical signal (red line), generated by the transmitter, to acoustic wave, and the pressure reflected from the imaging target is converted electrical signal (black line) by the transducer at the receiver (Rx) phase.

acoustic wave generated from the pulse propagates through a medium. The medium has certain mechanical or acoustic impedance,

$$Z_m = \rho c. \tag{1.3}$$

When the wave faces a material that has different Z_m, part of the wave continues to the material and the other part is reflected back at the boundary between the medium and the material which called echo signal. The echo signal travels back to the transducer, and it is converted to an electrical signal (Fig. 1.3). The electrical signal implies two important information: distance and the acoustic impedance of the material. Assuming that the wave has constant velocity for propagation because the wave had a round-trip, the arrival time is

$$t_{arrival} = \frac{2D}{c} \tag{1.4}$$

where D is the distance between the transducer and the material. Accordingly, the distance is calculated by

$$D = \frac{ct_{arrival}}{2}. \quad (1.5)$$

The echo signal has different amplitude based on acoustic impedance difference between the material and the medium, and the energy ratio between original signal and the reflected signal, which called reflection ratio, is calculated by

$$R = \left(\frac{Z_2 - Z_1}{Z_2 + Z_1}\right)^2 \quad (1.6)$$

where Z_1 and Z_2 are the acoustic impedance of the medium and the material respectively.

To create the image, the echo signal undergoes following steps. First, the signal amplified with low-noise amplifier (LNA) to reduce the effect of the noise in the following stages. Second, an envelope detector which extracts the amplitude of the signal to calculate the amount of energy in the signal, which is called A-mode (amplitude mode) scan. As explained above, because we know the acoustic impedance of medium (generally water), by calculating the energy, we can export the reflection ratio which implies the acoustic impedance of material. After one A-mode scan is done, the transducer is slightly rotated to acquire another A-mode scan line. The rotation and A-mode scan are repeated until it completes the scan of the entire cross section. The whole A-scans are mapped as brightness level (the higher amplitude, the brighter point), of the point, where the arrival time indicates, on the scan line. The image generated from the entire process is called B-mode (brightness mode) image. Since the system should wait for the arrival of the echo signal, the duration of the A-mode scan (Tx phase + Rx phase in Fig. 3) is determined by the required image depth. Since, if the duration is too large, frame rate drops, the duration should be carefully decided considering the tradeoff between imaging depth and frame rate.

The ultrasound imaging has the limitation of minimum separation between layers, which called spatial resolution, and there are two types of resolutions: axial and lateral resolution. The axial resolution is the minimum space along the radial axis, and the resolution is following

$$R_A = \frac{BW \times c}{2} \tag{1.7}$$

where BW is the bandwidth of the acoustic wave. The wider bandwidth makes the acoustic wave a single pulse, and it takes lower space along the radial axis. Hence, the higher bandwidth improves axial resolution. Since the wavelength of the wave is constant regardless of distance, the axial resolution is not changed along the axis. The lateral resolution is minimum space in a perpendicular to the radial axis. Because the wave is spread along the distance, the width of the beam, which determines the lateral resolution, is wider at the further distance. Since general ultrasound adopts beamforming, there is a focal point which has the narrowest width and the best lateral resolution. After the point, the width of the beam is increased with the further distance, and the lateral resolution is decreased. Therefore, the lateral resolution is expressed as

$$R_L = \frac{\lambda F}{D} \tag{1.8}$$

where D is the aperture size and F is a distance of the focal point from the transducer, which is called focal depth. In this equation, we have another important factor, f-number. The f-number refers ratio of the focal depth and aperture size (*F/D*).

1.4 Synthetic aperture imaging

As described above, the ultrasound provides a good image only around the focal point. Therefore, if the imaging depth and the number of scan line increase, the frame rate

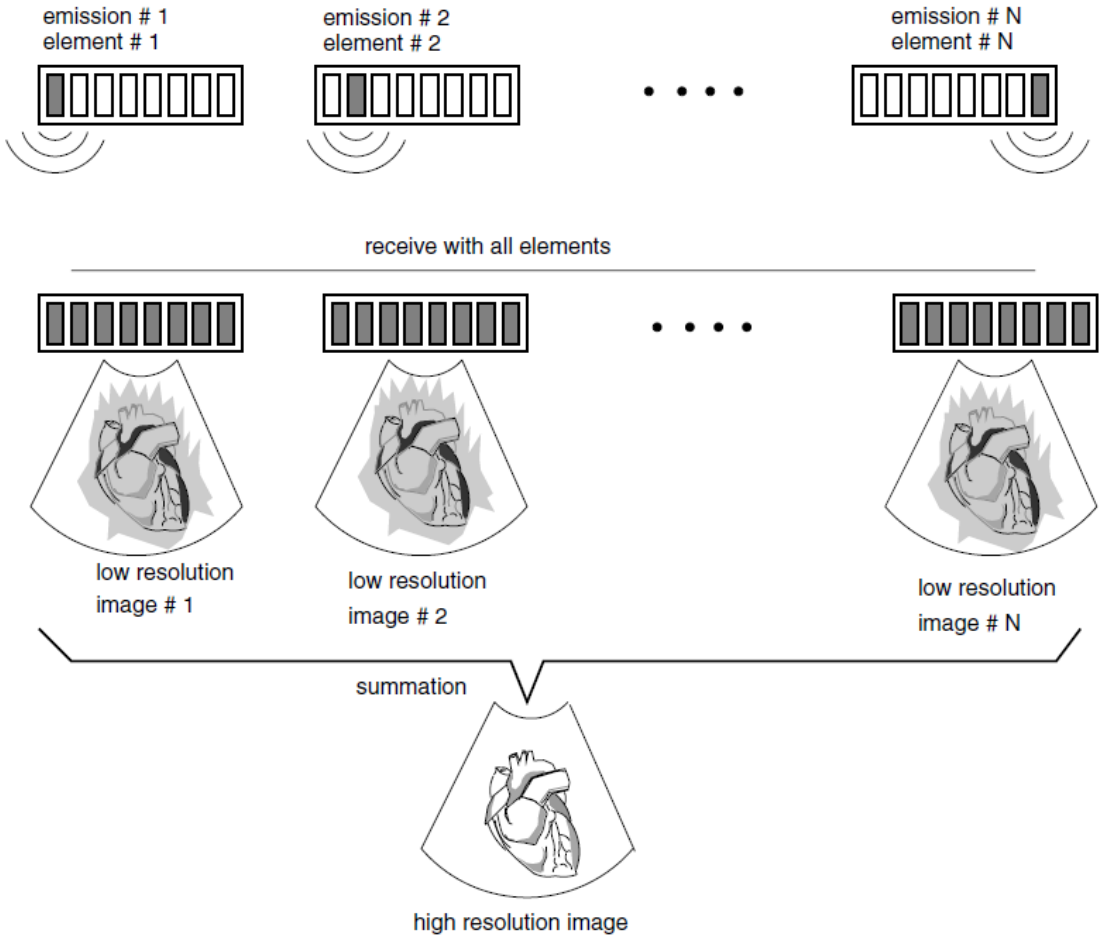


Figure 1.4. Basic operation of synthetic aperture imaging (adapted from [51]).

progressively lowers. Therefore, synthetic aperture imaging technique, which origin from the synthetic aperture radar (SAR), was introduced to address the problem. In SAR, the radar aperture is moved and synthesized, and the object is located in far-field. On the other hand, medical ultrasound imaging array is stationary, and the target is located in the near-field. Therefore, the array can rapidly measure the aperture [50].

The basic operation of synthetic aperture imaging is shown in Fig. 1.4. A single element transmits acoustic wave forward to the target and receives its echo signal, and the low-resolution image is acquired. Then, it repeats the same pulse-echo measurement by

varying Tx and Rx for all of the combinations. Considering the geometries of Tx and Rx elements, we can calculate the time position of the image point. After calculating time position of the all of the points, we can map the point into a low-resolution image. By combining all the low-resolution images from every element, a high-resolution image is acquired. Since it combines several images, the signal-to-noise ratio (SNR) is improved by

$$SNR(dB) = 10\,log_{10}\,N \tag{1.9}$$

where N is a number of low-resolution images.

CHAPTER 2. MODELING AND EQUIVALENT CIRCUIT OF CMUT

The capacitive micromachined ultrasonic transducer (CMUT), shown in Fig. 2.1, is divided into two operation mode: a transmitter (Tx) and receiver (Rx). In general, HV DC bias is applied on CMUT to increase linearity and sensitivity. On the other hand, HV DC bias decreases operating frequency and bandwidth. Tx CMUT generates acoustic wave when an electrical pulse is applied on top of HV DC bias. The wave hits the surface of CMUT, and it deforms the CMUT top electrode. The deformation causes capacitance difference, and it cause generates a current.

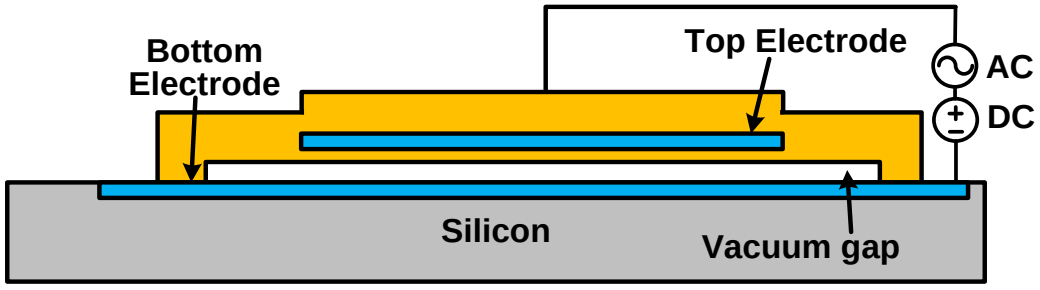


Figure 2.1. Cross section of the CMUT

In terms of an integrated CMUT transmit circuitry, because a pulser is generally designed to have a very low impedance to drive enough current, the performance of a CMUT is not affected by the driver circuit. As a receiver, a CMUT is usually modeled as a parallel resistor, capacitor, and a current source [52]. However, the current source is calculated based on the assumption that the input impedance of the transimpedance amplifier (TIA), a conventional front-end circuit of CMUTs, is small enough to neglect it. Considering that an imaging system needs a certain level of signal-to-noise ratio (SNR),

the TIA should have sufficient feedback resistance. Because the amplifier in the TIA has limited gain and bandwidth, the input impedance of the TIA may not be small enough to neglect. Thus, the performance of the CMUT does not follow the simulation results when the simple equivalent circuit is used. In addition, the behavior of the CMUT changes non-linearly with DC bias, complex acoustic cross talk from the neighbor elements should be accurately simulated. Thus, the simple equivalent mode, that consists of the parallel resistor, capacitor, and a current source, cannot sufficiently simulate stability and bandwidth of CMUT. We can use FEM simulation for the accurate behavior of CMUT, but it takes too much time and memory. Furthermore, we should simulate again whenever we change front-end circuitry. Those facts make FEM simulation nearly impossible to use for CMUT behavior. For those reasons, an accurate equivalent circuit of a CMUT array element that is compatible with circuit simulators including Spice and Cadence is required to get realistic simulation results.

Because small-scale ultrasound imaging applications have strict size limitations. Because external control signal needs extra wire connection and pad, it is better to avoid usage of external controls. Thus, we should optimize front-end circuitry with CMUT to avoid additional external compensation, and the equivalent circuit makes it possible.

We developed an MATLAB-based simulator that calculates bias dependent electrical impedance, static capacitance (C0), and transformer ratio [3]. We simulated a CMUT array with 40 MHz center frequency and 20 μm × 20 μm membrane dimensions, and we extracted the electrical impedance of the CMUT at different bias levels. We de-embedded C0 from the electrical impedance and fit the remaining impedance to a series

RLC circuit that models the peak of electrical impedance and a parallel RLC circuit that models the lower-frequency local peak of the impedance due to acoustic crosstalk.

We proposed a figure-of-merit (FoM) that is consisted of bandwidth, area, power consumption, and signal-to-noise ratio and evaluated the performance of transimpedance amplifiers that is front-end circuit of the system with different feedback network. From the results, we showed optimized TIA for the specific CMUT.

2.1 Small-signal modeling of receiver CMUT

Because of the nonlinear dynamic behavior of the CMUTs, accurate modeling of it is very important for demanding applications including tissue harmonic image [53], [54]. Therefore, we have developed the accurate nonlinear model of CMUTs including cross-coupling between elements in an array [55]. Although we prove the CMUT model can represent nonlinear behavior, it is limited for the CMUT without the front-end circuits. As we mentioned in the previous chapter, CMUT is vulnerable to parasitic, and the front-end circuits should be taken into account in the simulation of the CMUT array. Therefore, we developed the algorithm extracting the lumped model from our previous model[55].

The simulator proposed by Satir et.al. [55] (referred as a MATLAB-based simulator in the rest of the paper) is capable of transient simulation of any input voltage of the CMUT array with any termination. This flexibility can be utilized to extract the impedance values of the CMUT elements. The small signal equivalent circuit assumption is made when the CMUT devices are operating in receiver mode. As a result, the complex input electrical impedance across the frequency range of interest can be obtained by simply dividing the input voltage with the output current simulated at a certain DC bias.

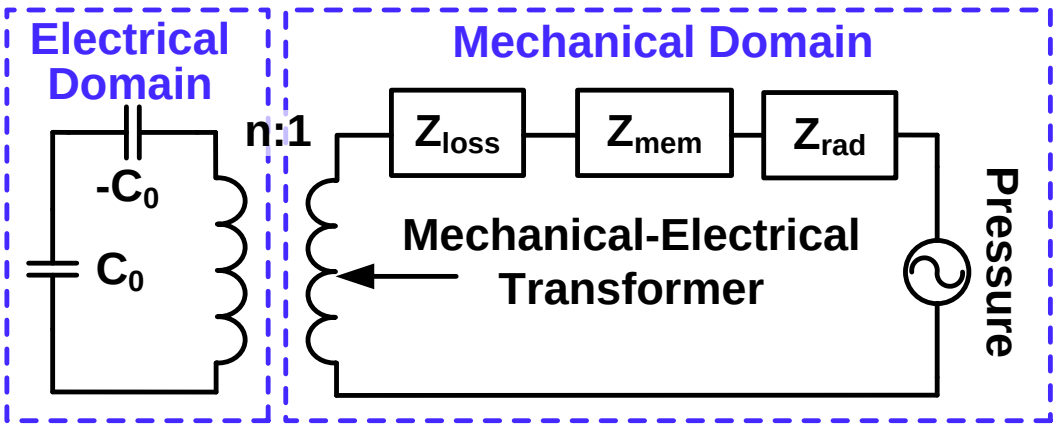
$$\varphi = \frac{I}{u} = \frac{F}{V} = \frac{2pA}{V} \tag{2.1}$$

Similarly, the transformer ratio (φ) can be obtained by applying an input force (F) and dividing the output current (I) to the velocity (u) the force generates at a certain DC bias. The transformer ratio can also be expressed as the ratio between force and voltage (V) as seen in (2.1). Therefore, the relationship between input pressure (p) and equivalent input voltage can be obtained by dividing with twice the CMUT area (A), since the incident pressure is doubled on the blocked CMUT surface. A short circuit termination along with Gaussian input voltages and forces were used to obtain the impedance and transformer ratios of the CMUT device at different DC bias level.

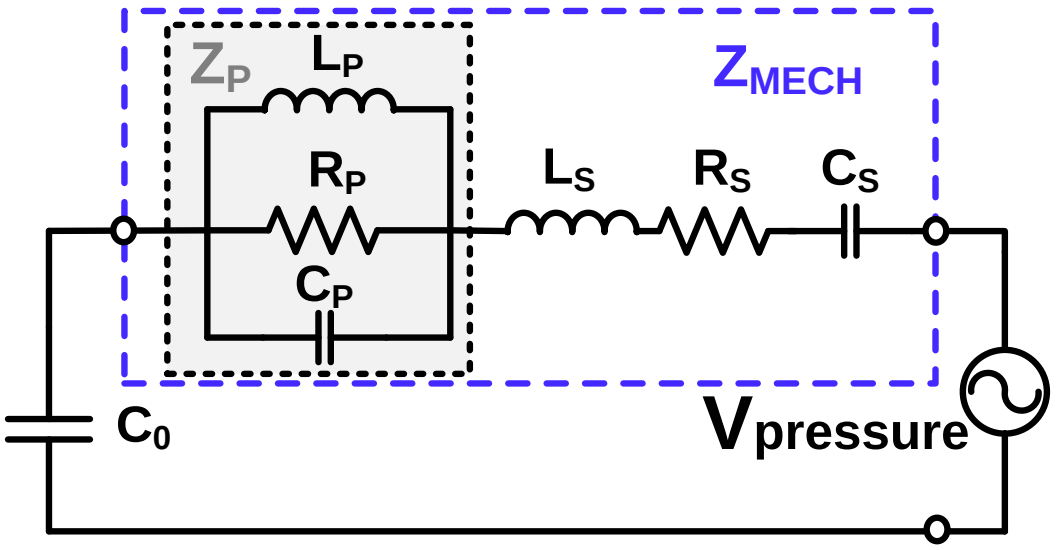
As shown in Fig. 2.2a, conventional CMUT equivalent circuit follows Mason's parallel plate transducer model [52] which consists of a mechanical port, an electrical port, and a transformer that connect these two ports. Since the purpose of the equivalent circuit is making the transducer model viable at electronics side, we simplified the model by transferring all the parts in the mechanical domain to the electrical domain by using the transformer ratio. Then, we combined all the components except for C_0 and the pressure generated voltage source in an impedance (Z_{MECH}), and the equivalent model is simplified to a simple three-component model, as shown in Fig. 2.2b.

In this study, we used a 1-D CMUT array that has a center frequency of 40 MHz and -3dB bandwidth of 30 ~ 45 MHz (Fig. 2.3). The CMUT array has 12-elements that are consisted of 40 membranes. The size of each membrane is 20 μm × 20 μm with 25 μm pitch. We simulated impedance of CMUT with different DC bias, shown in Fig. 2.3. When we increase DC bias, the amplitude of the impedance increase and resonant frequency

decrease.



(a)



(b)

Fig. 2.2. (a) CMUT equivalent circuit based on Mason's parallel plate transducer model, and (b) simplified three-port CMUT equivalent model.

Unlike single parallel plate transducers, the CMUT shows two peaks at the impedance. The

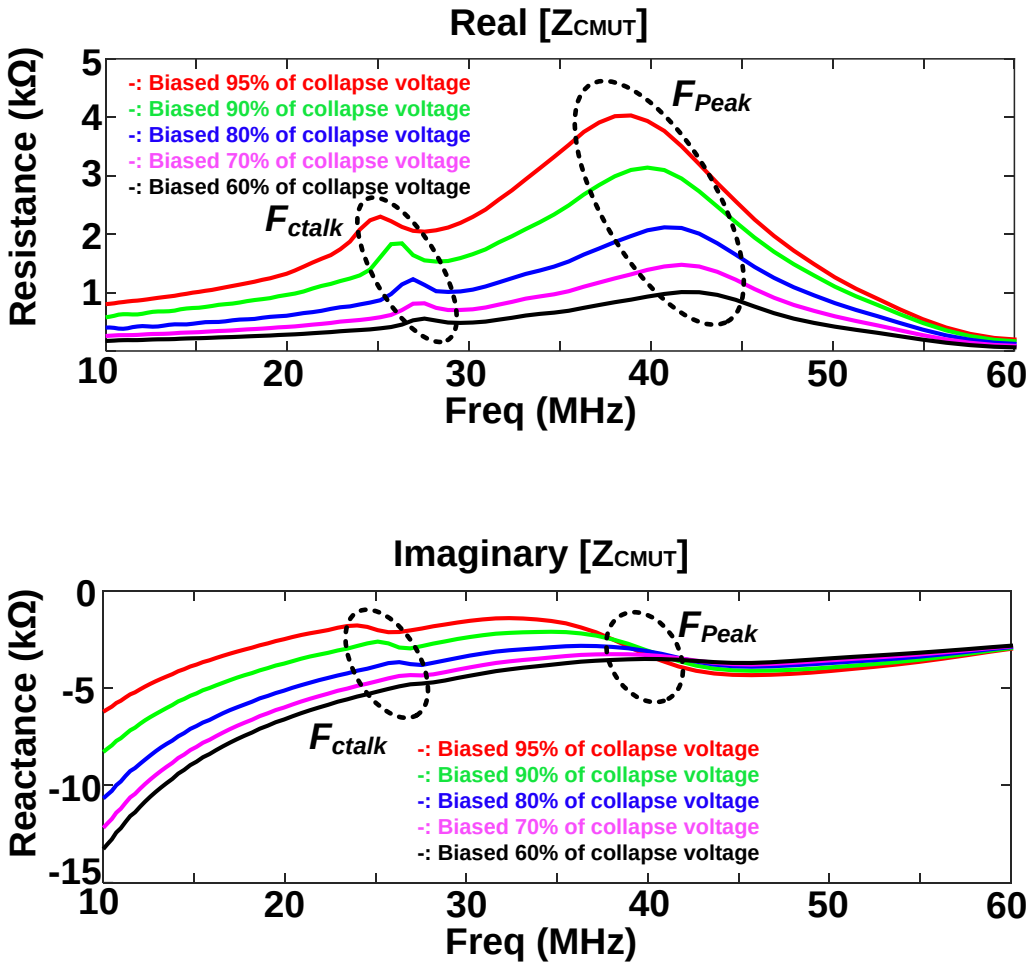


Figure 2.3. Impedance of the target CMUT with different DC bias.

main peak at 40 MHz (F_{peak}) is due to resonance of CMUT, and the lower peak at 28 MHz (F_{ctalk}) is due to acoustic cross talk from the neighbor elements. We empirically modeled the acoustic crosstalk as parallel RLC (Z_P in Fig.2.2b) and main resonance as series RLC

As the first step of modeling, we calculated C_0, CMUT impedance, and transformer ratio from the MATLAB based simulator. Because we know C_0 value, we can de-imbed C_0 from the CMUT impedance by

$$Z_{MECH} = \frac{1}{\frac{1}{Z_{CMUT}} - sC_0} \tag{2.2}$$

Series L_S and C_S do not have contribution at real part of Z_{MECH} (R_{MECH}), and, except for nearby F_{ctalk}, Z_P has limited effect on R_{MECH}. Consequently, we choose the average of R_{MECH} as an initial point of R_S. On the other hand, at F_{ctalk}, R_{MECH} is the same as R_S+R_P, which can give the initial value of R_P. As shown in Fig. 2a, the peak of R_{MECH} at F_{ctalk} is very narrow and the effect of it is negligible at F_{peak}. Therefore, F_{peak} can be expressed as

$$F_{peak} = \frac{1}{2\pi\sqrt{L_S\frac{C_0C_S}{C_0+C_S}}} \tag{2.3}$$

, and we can re-order the equation to

$$L_S = \frac{1}{4\pi^2F_{PEAK}^2}\frac{C_0+C_S}{C_0C_S}. \tag{2.4}$$

Since, at F_{ctalk}, C_P and L_P are resonating and canceled,

$$Z_{MECH} = R_P + R_S + \frac{1}{sC_S} + sL_S. \tag{2.5}$$

By substitute L_S with (4),

$$C_S = \frac{\frac{1}{s_{ctalk}} + \frac{s_{ctalk}}{4\pi^2F_{PEAK}^2}}{Z_{MECH} - R_P - R_S - \frac{s_{ctalk}}{4\pi^2F_{PEAK}^2C_0}} \tag{2.6}$$

where $s_{ctalk}=j\cdot 2\pi\cdot F_{ctalk}$. Because all of the variables are calculated in the previous steps, we can calculate C_S and L_S from (2.6) and (2.4) respectively. Now, all the initial values except for C_P and L_P are derived, and we can calculate Z_P from Z_{CMUT}. Z_P can be derived as

$$Z_P = \frac{\frac{1}{C_P}}{s^2+\frac{s}{C_P R_P}+\frac{1}{C_P L_P}}, \tag{2.7}$$

and, based on the basic 2nd order circuit theory, we can derive C_P and L_P with a calculated bandwidth of Z_P by

$$C_P = \frac{1}{2\pi \times Bandwidth \times R_P}, \tag{2.8}$$

$$L_P = \frac{1}{4\pi^2 F_{Ctalk}^2 C_P}. \tag{2.9}$$

Now, we got all the initial values of each component. To improve the accuracy of it, we run following iteration steps. Because the most important part of the model is matching at F_{peak}, which is operating frequency, we calculate C_S with initial values of other components by

$$C_{Scal} = \frac{1}{s(Z_{MECH} - sL_S - R_S - Z_P)} \quad . \tag{2.10}$$

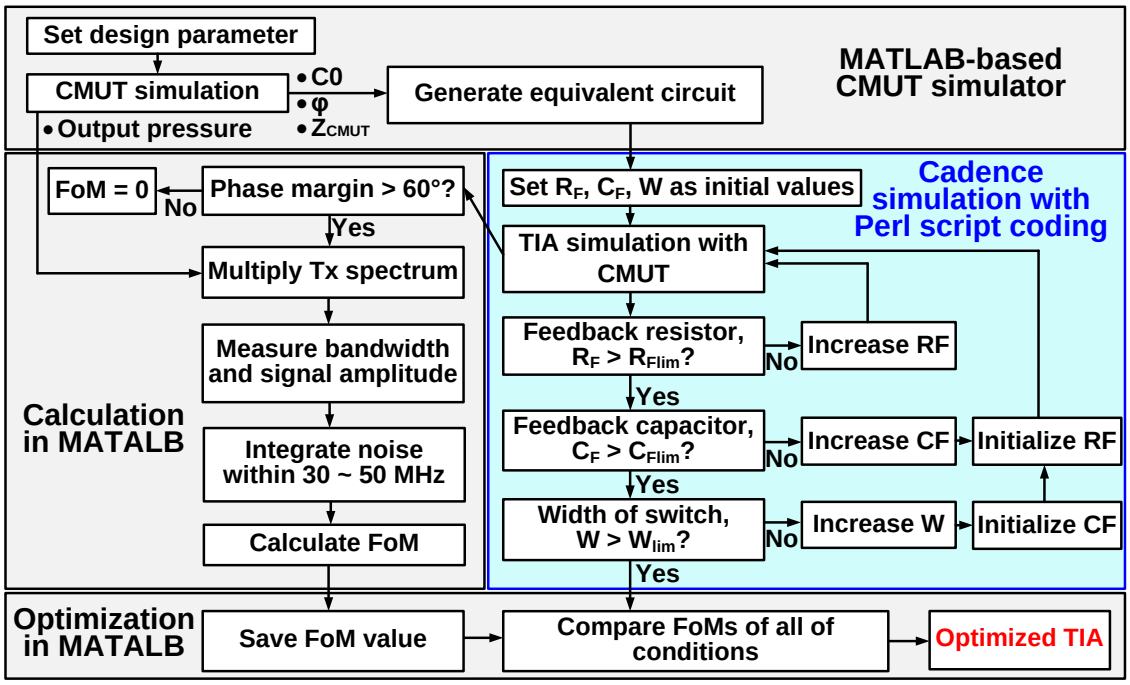
Because initial value of R_S is the rough value, calculated C_S (C_{Scal}) can be complex number, and we divide effect on R_S from C_{Scal} by

$$R_S = R_S - \frac{w_{peak}^2 \times Imaginary[C_{Scal}]}{\left(w_{peak}|C_{Scal}|\right)^2} \tag{2.11}$$

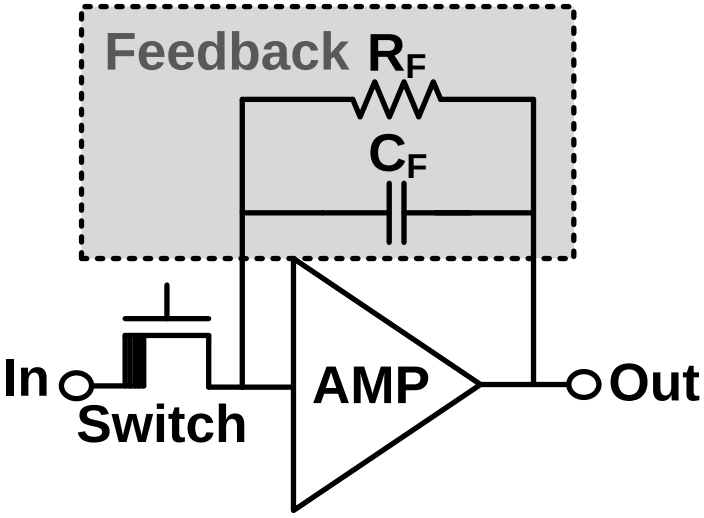
$$C_S = \frac{\left(w_{peak}|C_{Scal}|\right)^2}{w_{peak}^2 \times Real[C_{Scal}]}. \tag{2.12}$$

From the new calculated C_S and L_S (calculated from (2.4) with new C_S), we repeat the steps from (2.7) to (2.12).

2.2 Design procedure of transimpedance amplifier



(a)

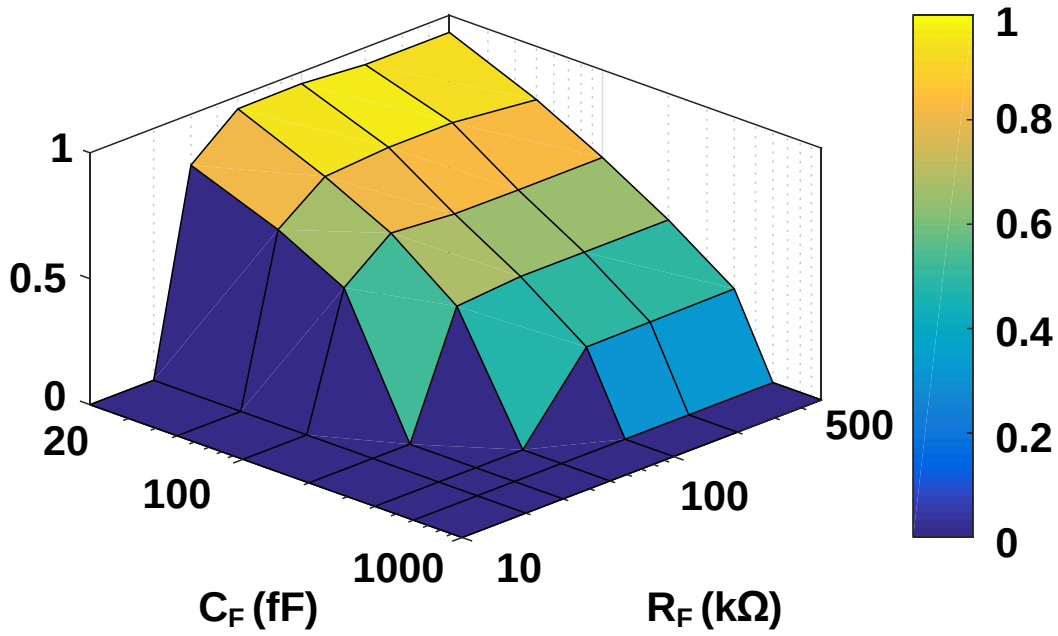


(b)

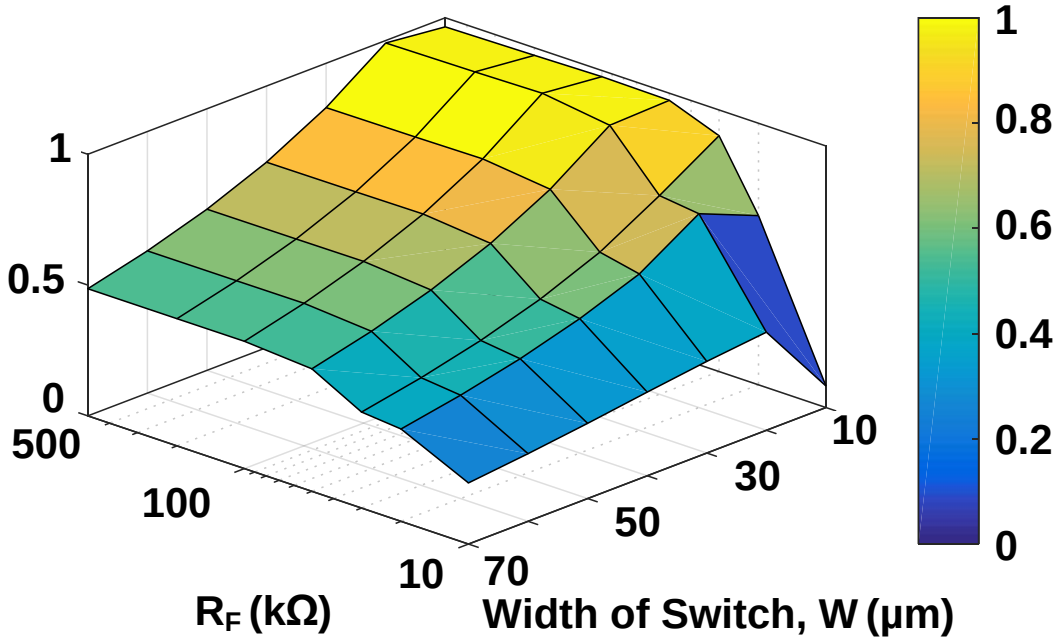
Figure 2.4. (a) Design procedure and (b) structure of transimpedance amplifier. C_{Flim} , R_{Flim}, W_{lim} are upper boundaries of C_F, R_F, and W respectively.

A transimpedance amplifier (TIA) is the most common front-end circuit of CMUTs. Although there is a study to optimize the TIA for CMUT [56], the study was limited to the simple RC model of CMUT, which cannot represent CMUT's nonlinear behavior. To address the challenge, modeling of linear acoustic radiation and crosstalk effects based on the boundary element method was suggested in [91]. However, it is too complex to used in circuit simulation, and we suggest an modeling of CMUT array on lumped RLC model and iterative design procedure with the model to optimize the TIA for the specific CMUT (Fig. 2.4). To simplify the procedure, we confine the design variation on feedback and design the amplifier which has more bandwidth (~80MHz) than the CMUT bandwidth.

Although stability does not harm the performance of the TIA if sufficient phase margin is guaranteed, but, if not, TIA cannot correctly receive the signal. Since the stability simulation should consider parasitic, it requires accurate circuit simulator like Cadence. Therefore, to improve the accuracy of the simulation, we linked MATLAB, which extracts the equivalent model from the MATLAB-based simulator results, and Cadence, which simulates signal and noise with the circuits and the model, by using Perl script. At the first time, MATLAB- based simulator run a simulation for the CMUT behavior. Since every element in the CMUT array in this study shares bottom electrode to reduce fabrication complexity, bias for Tx and Rx CMUTs are always the same, and MATLAB-based simulator runs Tx-Rx simulation at the same time. Based on Rx simulation results we generated equivalent circuit of CMUT element by using the algorithm we described above, and the equivalent circuit is transferred to the Cadence. In Cadence, we set series / parallel RC as a feedback and run phase margin, AC response, and noise simulation with every corner conditions, which are transferred to MATLAB. Based on the data, first of all,



(a)



(b)

Figure 2.5. Normalized FoM with (a) R_F versus W (C_F = 0) and (b) C_F versus R_F (W= 20μm).

stability (>60° phase margin secures stable operation) was checked, and, if the feedback does not satisfy it (at least one of corner condition), we made the FoM=0. Once the stability is satisfied, the spectrum of Tx pressure, which calculated in the MATLAB-based

simulator, is multiplied on the AC response of TIA that gives a complete pulse-echo spectrum of the specific CMUT. Signal and noise power are calculated from the spectrum in the range of 30-50 MHz which is the bandwidth we are interested in. For the sake of comparison, we set the figure-of-merit (FoM)

$$\mathrm{FoM} = \frac{\mathrm{Signal}\times\mathrm{Bandwidth}}{\mathrm{Noise}\times\mathrm{Area}\times\mathrm{Power}}. \tag{2.13}$$

Signal and bandwidth can improve image quality and resolution, but noise power and area decreased image quality and increased the size of the system. Since the amplifier (AMP), which is already designed prior to the optimization procedure, is the only active component, which consumes power, power consumption is identical in every condition, and the power consumption has no effect on FoM in this procedure. We run whole procedure for every feedback capacitor (C_F) and resistor (R_F) and width of the switch (W) in the boundaries which set to include the optimal point.

Based on simulation results, we export the data and transfer them to MATLAB. MATLAB calculates FoM and compares FoM of all of the different conditions. Because, in TowerJazz 0.18-μm HV CMOS process that is used in this optimization, a resistor with larger than 500 kΩ and a capacitor with larger than 2 pF take the too large area to fit in required size, we set a boundary within those values. Since the CMUT is operating at 80-90% of collapse voltage (V_{col}), we run two set of simulations with 80% and 90% of V_{col} separately and combined the results to compare. As shown in Fig. 4, R_F= 100kΩ without C_F shows the best FoM and all the series R_F-C_F in the boundaries could not meet the stability requirement. Consequently, we choose resistive feedback TIA with 100 kΩ feedback resistor.

CHAPTER 3. IMPULSE RADIO PULSE WIDTH MODULATOR

Classic analog to digital converters (ADC) have been at the heart of almost every modern data acquisition (DAQ) systems since 1970's and still constitute an active and thriving field with a wide variety of architectures and a large number of publications and patents each year [57]. However, when it comes to certain applications with high data throughput and extreme size and power constraints, they may not represent the best choice. One of these applications is vascular ultrasound imaging, in which the ultrasonic transducers and their interfacing circuitry should fit at the tip of 3 - 8.2 French (F) catheters (1 mm – 2.7 mm in diameter) [58], [13]. Yet there is an effort underway to combine capacitive micromachined ultrasound transducers (CMUT) with high voltage (>60 V) readout circuitry at the tip of 1.1 F - 2.67 F guidewires (0.36 mm – 0.89 mm in diameter) to measure stent deployment or an artery wall diameter [59].

The acoustic pulse echo signal generated by a high-frequency CMUT occupies the 35 – 45 MHz spectrum [59], which after down-conversion to baseband would still need a sampling rate of at least 10 MS/s. Due to lack of space, interface electronics for piezo and CMUT transducers have traditionally been limited to transimpedance amplification (TIA), buffering, and delivery of the amplified signals across the catheter with a bundle of thin wires, one for every channel, and digitization outside the patient body. There has been attempts to time-division multiplex (TDM) the analog signals [60], [61] or use optical readouts [62] with limited success. However, to the best of our knowledge, no one has been able to include an ADC on the catheter. As a result, there has always been a compromise between the number of channels, the diameter of the catheter, resolution of the image, and

its field of view. Aside from finding a way to deliver the acquired wideband data out of the body, a potential remedy for reducing the number of wires towards a thinner catheter is to send the data wirelessly over the short distance from inside the heart to a receiving patch antenna attached to the skin on of the patient's chest (~10 cm).

We propose the use of analog to time conversion (ATC) in lieu of traditional ADC in the abovementioned DAQ applications and present a new architecture based on a combination of ATC, impulse radio, and time-to-digital conversion (TDC) that would go one step further and satisfies the strongly preferred wireless data communication approach, particularly in biomedical applications, by creating a wireless DAQ (WDAQ). Some of the advantages of the ATC over the conventional ADC approach are: First, since the ATC architecture is simpler than most ADC architectures, it occupies a smaller area on the chip in a given process and consumes considerably less power than high-speed ADC architectures [63]. In fact, the ATC can be considered the analog half of the well-known family of integrating ADCs, such as single- and dual-slope ADCs. However, the digital half, in this case, is pushed onto the receiver (Rx) side, where size and power are not nearly as much constrained, reducing the area and power requirement on the transmitter (Tx) side [63]. Moreover, the ATC does not require a high-frequency clock, further reducing the dynamic power consumption in digital blocks, while creating a less noisy environment in system-on-a-chip (SoC) implementations. The total capacitance required for implementing an ATC block is considerably less than low power ADC architectures, such as successive approximation register (SAR), resulting in more area saving particularly in processes that do not have a large number of metal layers [64]. Moreover, ATC is not as sensitive to matching among small capacitors as SAR-ADC [65]. Considering that ATC involves

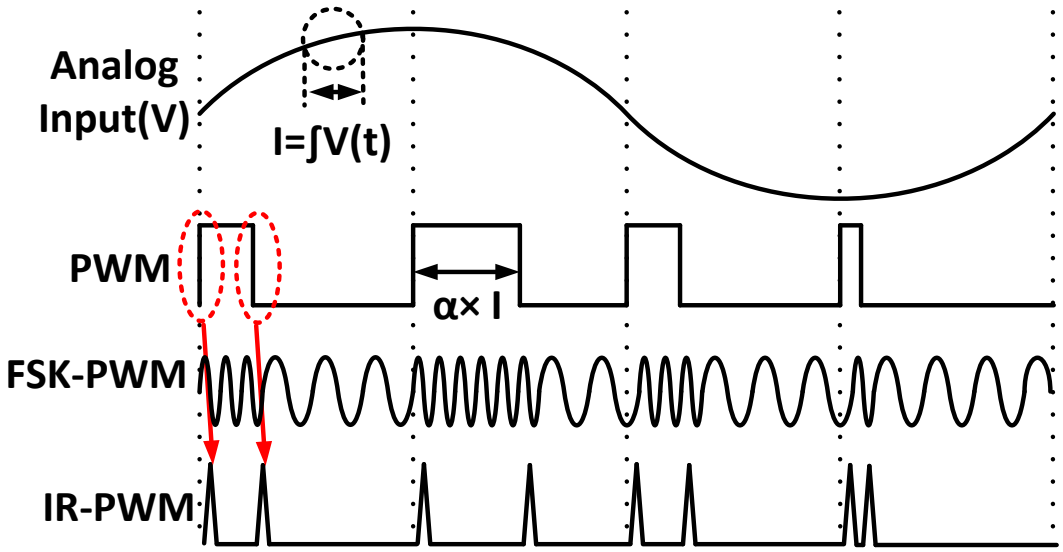


Figure 3.1. Operational diagram of pulse width modulated impulse radio (IR-PWM) wireless data acquisition (WDAQ). The information in the analog input signal (V) is converted into a pulse with the width of α × I. In FSK-PWM, a frequency-modulated sinusoidal wave is transmitted with two frequencies that represent '1' and '0' of the PWM pulse. In IR-PWM, sharp impulses are transmitted at every rising and falling edges of the PWM signal.

integrating charge over the period of each sample, it inherently reduces high-frequency noise compared to multiple charge redistributions in SAR-ADCs. Finally, we have shown in [66] that wirelessly transmitting the PWM signal, which results from the ATC, over a short distance can be considerably more power efficient than a serial data bit stream that results from the conventional ADC approach.

In our earlier implementations of the ATC-WDAQ, we used frequency-shift keying (FSK) to establish the wireless data link [63]. However, the voltage controlled oscillator (VCO) requires considerable power and area. Since the IR-PWM substitutes the carrier signal with narrow impulses, the Tx power efficiency would be considerably higher, while the simple IR-UWB architecture saves silicon area. In the conventional IR-UWB digital communication, three encoding techniques are widely used: binary phase shift keying (BPSK), on-off keying (OOK), and pulse position modulation (PPM). The BPSK and PPM

change the polarity and timing of the impulses for ‘0’ and ‘1’ in every bit of data, respectively, while the OOK only sends an impulse when the data is ‘1’. Considering that most of the power consumption would be in the PA and assuming that the probabilities of ‘1s’ and ‘0s’ in a serial data bit stream are equal, the expected number of the transmitted impulses in OOK would be half of BPSK and PPM, resulting in cutting the Tx power consumption almost in half. On the other hand, the IR-PWM transmits only two impulses for each sample, as shown in Fig. 3.1, representing N data bits, where N is the ATC resolution. As a result, the Tx power in IR-PWM is only 1/N of the BPSK and PPM, and 2/N of the OOK [66].

3.1 IR-PWM Architecture

To define the design specifications for the proof-of-concept WDAQ prototype, we have considered the fact that vascular ultrasound imaging, our exemplary application, requires 50 dB signal-to-noise ratio (SNR) on integrated echo signal data for 40 dB dynamic range image [67]. By adopting a method known as synthetic aperture imaging, the required SNR can be reduced to 35 dB with a 6-element array [68]. Considering the CMUT readout required a sampling rate of 10 MS/s [59], the dual-slope charge sampling (DSCS) analog front end (AFE) presented in [69] (Fig. 3.2), which was designed for sampling rates in the order of 1 MS/s, was not be sufficient. However, it was the basis of the new design.

The operation of the DSCS-AFE in Fig. 3.2a is shown in Fig. 3.2b. Briefly, during the pre-charge phase (Φ1), *CAP*+ and *CAP*- are pre-charged to V_{REF+} and V_{REF-}, respectively. During the evaluation phase (Φ2), *CAP*+/*CAP*- are charged/discharged by

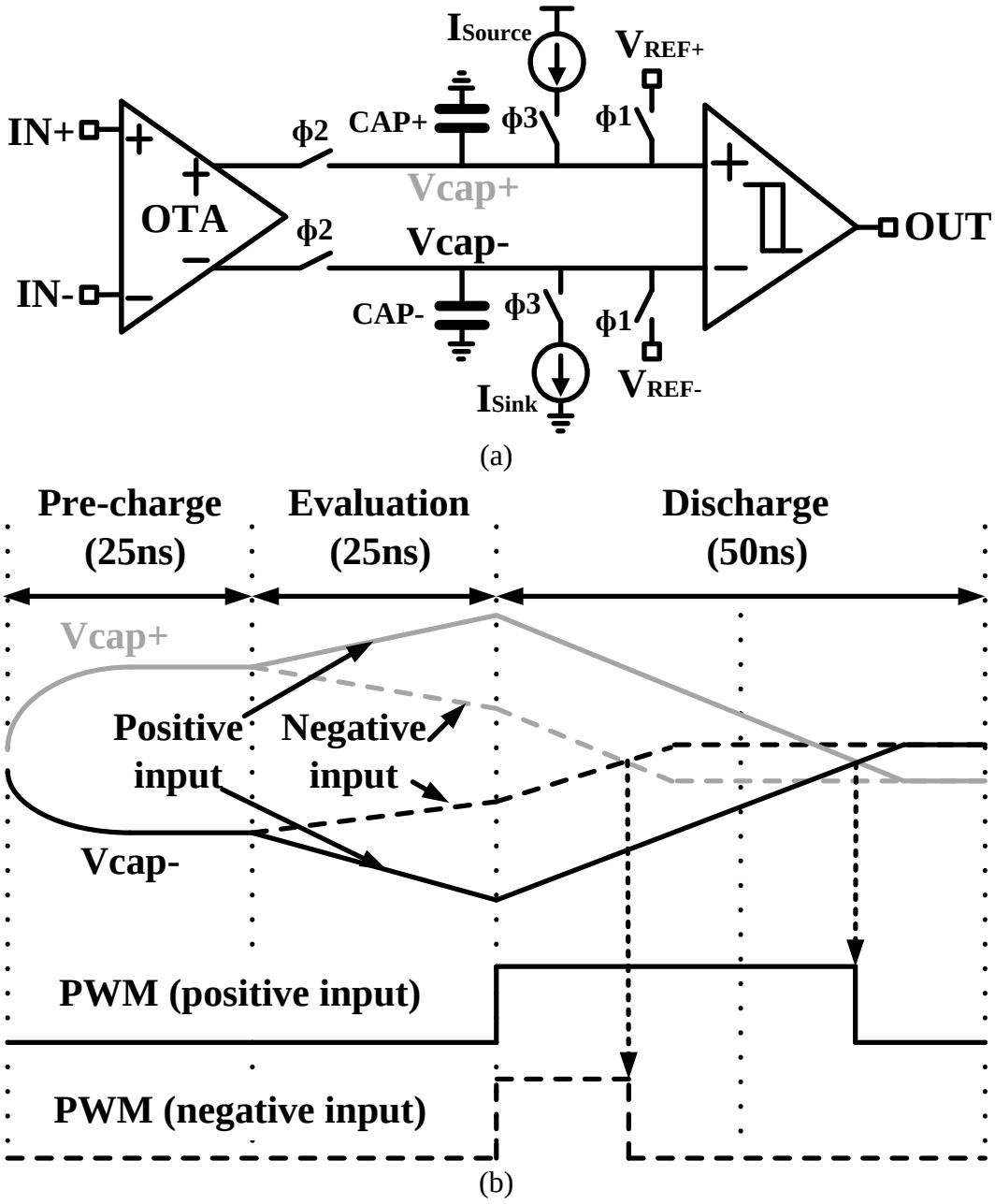


Fig. 3.2. (a) Schematic and (b) timing diagrams of the dual-slope charge sampling AFE [69].

the OTA at a rate proportional to the input voltage. During the discharge phase (Φ3), I_{source}/I_{sink} discharge/charge *CAP+*/*CAP-* at a constant rate, while a hysteresis comparator that sets at the beginning of this phase, generates the PWM pulse. To achieve high sampling rate, settling times of the OTA and current sources need to be considered. In addition,

increasing the sampling rate exacerbates the effects of charge injection and clock feedthrough on V_{CAP+} and V_{CAP-}, which are directly related to the ATC noise performance. The amount of charge injection noise can be found from,

$$V_{inj} = \frac{WLC_{ox}}{C_{CAP+}}(V_{DD} - V_{TH}), \tag{3.1}$$

where C_{ox}, V_{TH}, W, and L are the gate capacitance per unit area, threshold voltage, width, and length of the MOS switches, respectively [70]. From [71], the clock feedthrough noise is given by,

$$V_{feed} = \frac{WLC_{ox}}{2C_{CAP+}}(V_{DD} - V_{SS}). \tag{3.2}$$

which indicated that to minimize noise, W and L of the switches should be minimized, while *CAP*+/*CAP*- should be maximized. On the other hand, since *CAP*+/*CAP*- charging/discharging currents pass through these switches, their ON-resistance should be reduced by increasing their widths. Moreover, the OTA output current should be small to reduce power consumption and the undesired voltage drop across these switches. *CAP*+/*CAP*- should also be small to achieve sufficient sampling rate by charging and discharging rapidly. These are conflicting requirements that limit the DSCS-AFE performance.

3.2 Triple-Slope Pulse Width Modulation

To address these issues, we have designed a triple-slope pulse width modulation (TSPWM) scheme, shown in Fig. 3.3a, in which switching functions have been transferred from the OTA output to its input. Consequently, the OTA also takes over the role played

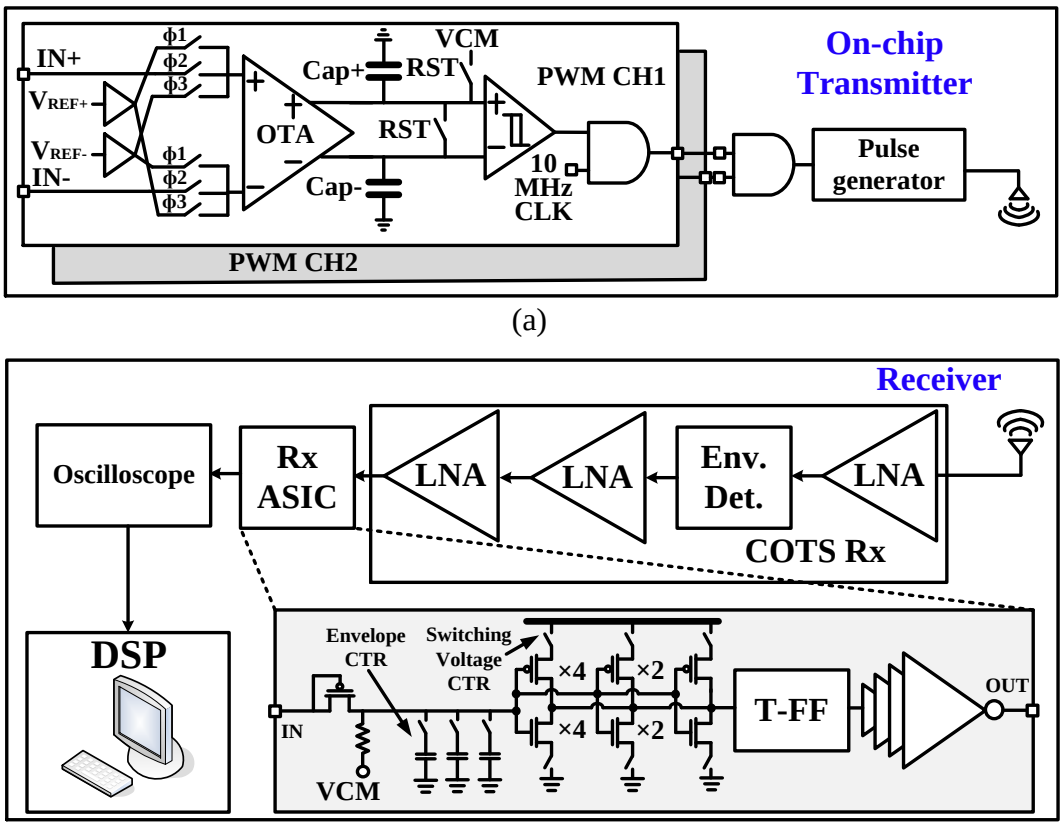


Figure 3.3. (a) Schematic of the proposed IR-PWM transmitter and (b) receiver.

by I_{source} and I_{sink} in DSCS. Fig. 3.4 shows the timing and operation of the new TSPWM, which is divided into three phases. In the pre-charge phase (Φ1), a positive reference voltage, $V_{REF} = V_{REF+} - V_{REF-}$, is applied to the OTA differential input, resulting in the OTA increasing the voltage difference between V_{CAP+} (ascending) and V_{CAP-} (descending) from the OTA common-mode voltage, *VCM*. In the evaluation phase (Φ2), the OTA input is connected to the differential input voltage, V_{IN}, converting it to a proportional pair of currents that charge/discharge *CAP+*/*CAP-*, respectively. Finally, in discharge phase (Φ3), a negative reference voltage, $-V_{REF} = V_{REF-} - V_{REF+}$, is applied to the OTA, resulting in the voltage difference between V_{CAP+} (descending) and V_{CAP-} (ascending) to decrease down to zero, where we refer to as the 'end point'. At the end point, the comparator, which was

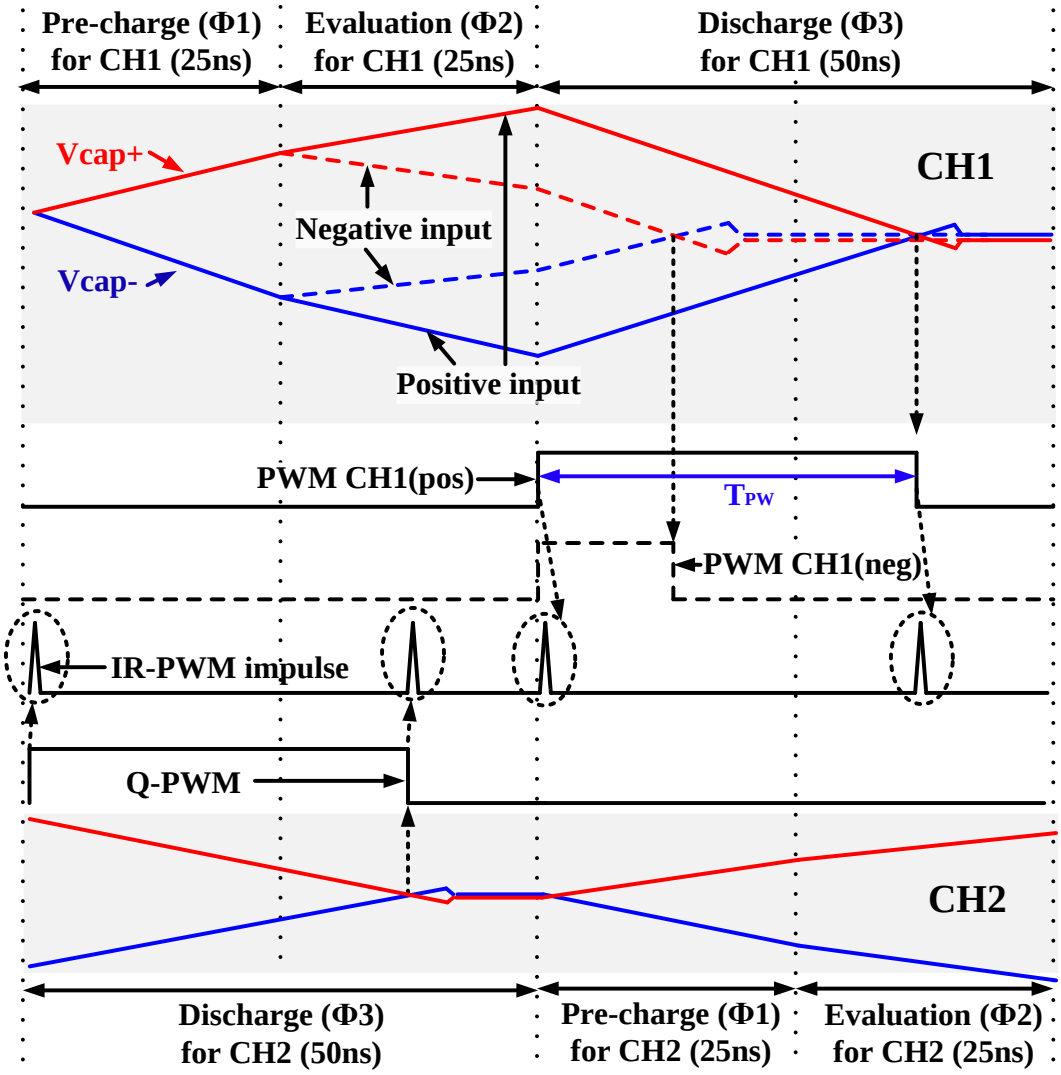


Figure 3.4. Timing diagram of the proposed triple-slope charge sampling IR-PWM.

turned on with its output set at the beginning of Φ3, is reset to generate a PWM pulse along with the RST signal, which returns the TSPWM circuit back to the initial state by setting *CAP+*/*CAP-* at *VCM*, turning off the comparator, and zeroing the differential OTA input, i.e. connecting them to *VCM*.

The time it takes from starting of Φ3 to the end point is measured as the PWM pulse width, T_{PW}, which contains analog sample information. Since T_{PW} only occupies Φ3, which

is chosen to be 50 ns, i.e. half of the total sampling period, Φ1 + Φ2 can be used by an identical TSPWM AFE, which can share the same communication channel via time division multiplexing (TDM), as shown in Fig. 3.4 timing diagram, to double data throughput. To avoid interference between consecutive IR-PWM impulses (Fig. 3.4), a mask is used to limit T_{PW} to 44 ns, using a non-overlap clock generator.

Since the main switching activities are transferred to the OTA input and driven by buffers, the switching noise does not directly affect the sampling capacitors. Nonetheless, noise at the input of the OTA should also be lowered to improve the overall noise performance. The effect of added buffers are twofolds: low impedance termination for the switch and fast recovery of the OTA input voltage. When a switch has low impedance terminal, injected charge from the switch mostly flows into that terminal, preventing large variations in the high impedance OTA input. Moreover, the buffer reinforces the OTA input voltage rapidly every time the switch closes and reduces the switching noise. Because of this fast recovery, the spectrum of the switching noise is pushed to higher frequencies, where it is attenuated by the low-pass filtering and charge integration effects of the OTA and sampling capacitors, respectively.

Considering that charge variation from the onset of Φ1 to the end point is zero, the relation between T_{PW} and differential input voltage, V_{IN}, can be expressed as,

$$t_{\Phi 1} G_m V_{REF} + \int_0^{t_{\Phi 2}} G_m V_{IN}(t)\, dt - T_{PW} G_m V_{REF} = 0, \tag{3.3}$$

where G_m is transconductance of the OTA, $t_{\Phi 1}$ and $t_{\Phi 2}$ are the duration of Φ1 and Φ2 respectively, and TPW is PWM pulse width. Since $t_{\Phi 1} = t_{\Phi 2}$,

$$T_{PW} = t_{\Phi 1} + \frac{\int_0^{t_{\Phi 2}} V_{IN}(t)\, dt}{V_{REF}}. \quad (3.4)$$

Because $t_{\Phi 1}$, $t_{\Phi 2}$, and V_{REF} are a pre-defined value, V_{IN} is calculated from T_{PW}. Since, if V_{REF} is smaller than the dynamic range of V_{IN}, the T_{PW} exceeds the valid range, V_{REF} has to be larger than the input dynamic range of the PWM. In addition, if the dynamic range is too smaller than V_{REF}, the PWM output dynamic range is limited and it requires a high resolution of the TDC. Accordingly, the proper reference voltage determines the resolution of the PWM. To send T_{PW} to a receiver, we send impulses at the beginning and end of T_{PW}. The delay from the capacitor-loaded inverter and logic gates generates impulses at every edge of PWM signals (Fig. 3.2).

Since the sampling capacitors integrate the charge for 25 ns, it filters out the high-frequency signal with -3 dB bandwidth of

$$\frac{1.42}{2\pi t_{\Phi 2}} = 9.04\ MHz \quad (3.5)$$

where $t_{\Phi 2}$ is the duration of Φ2 [72]. Since the sampling rate of the PWM is 10 MS/s, the PWM cannot sample the signal higher than 5 MHz based on the Nyquist theorem. Therefore, the low-pass filtering function of the PWM does not limit the signal bandwidth.

3.3 IR-PWM transmitter

The IR-PWM is comprised of the reference voltage generator, the OTA, the comparator, and pulse generator (Fig. 3.3). The reference voltages (V_{REF+}, V_{REF-}, and *VCM*) are generated from the resistive voltage divider and driven by three individual buffers. To reduce the switching noise on the reference voltage, on-chip capacitors of 3 pF are used at

each buffer output. To increase the linearity of the OTA, the source degenerated differential input pair is used (Fig. 3.5a). Since the OTA directly drives *CAP*+ and *CAP*- which have variation in voltage two-stage OTA that isolates the input device from large voltage variation is used. The cascode at the second stage minimized the current variation from drain voltage (V_{OUT+} and V_{OUT-}) variation, and the first stage cascode increase the accuracy of the current mirror. Since decision making of the comparator in the PWM is not a clock-based work, the dynamic comparator that is commonly used in the ADC is not suitable. Therefore, we adopted a comparator with a source-coupled differential pair (Fig. 3.5b). Although the comparator has a positive feedback, it has nanosecond range delay. Considering that the maximum pulse width of the PWM signal is less than 50 ns, the delay significantly reduces the PWM output dynamic range. Since, at Φ3, $V_{CAP+,}$ and V_{CAP-} are changed with fixed slope, the comparator input-to-output delay is constant. Therefore, we set the intentional offset at the input of the comparator to compensate the delay. To save the power consumption in the comparator, the enable switch (*EN*) is used to make the comparator turn off when it is not used.

Fig. 3.5c shows the pulse generator that transmits impulses at rising and falling edge of the PWM signal. An inverter followed by capacitor bank delays the PWM signal, and a XOR gate consists of inverters and NAND gates generates sharp impulses with a pulse width of the delay. The impulse is applied to an all-digital power amplifier (PA) that drives an antenna. To adjust the spectrum of the transmitting impulse, we implemented a register and capacitor bank to change the inverter delay. The size of the inverter chain was set to achieve more than the output power of 0.2 mW with 50 Ω load (antenna load) which is the requirement for the application in [59].

3.4 IR-PWM Receiver

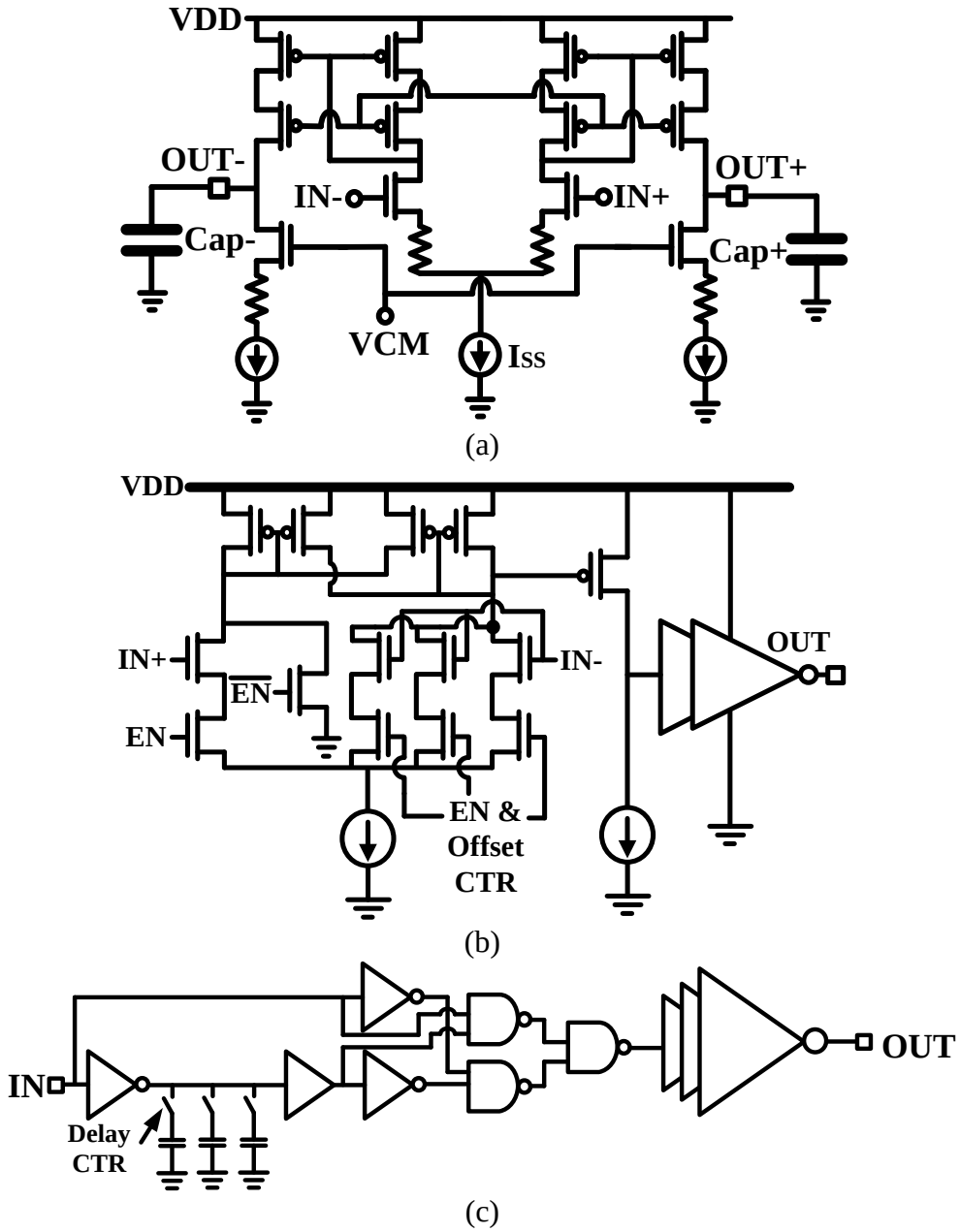


Figure 3.5. (a) Schematic diagrams of the OTA, (b) comparator with source-coupled differential pair, and (c) pulse generator.

We designed an IR-PWM Rx with commercial off-the-shelf components (COTS) and a custom designed printed circuit board (PCB). We used three LNAs (ADL 5542,

Analog device), which has individual 20 dB gain with a bandwidth of 0.5 ~ 6 GHz, and the envelope detector (ADL 5511, Analog Device), which have the input frequency range of 0 to 6 GHz (Fig. 3.3). The Rx antenna receives the pulse signal transmitted from the Tx, the LNA amplifies the received signal, the envelope detector down converts amplified signal, and the following LNAs amplify the envelope signal. We designed a Rx ASIC that converts the amplified envelope signal to a PWM signal. A diode connected PMOS and a capacitor remove undesirable pulses to prevent glitches, a size adjustable inverter that controls its switching voltage converts the analog impulse to a digital pulse, and a T-flipflop followed by a digital buffer recover to a PWM signal. The PWM signal is recorded by a digital oscilloscope (TDS-5054, Tektronix), and it is decoded in the MATLAB.

3.5 Noise Considerations in IR-PWM

In this section, by defining the noise source and showing how to convert the noise to a pulse width error, we present the design guideline and how much resolution it can achieve. Except for the input signal noise, IR-PWM noise composes of four parts: OTA, comparator, clock jitter, and receiver noise.

3.5.1 Operational transconductance amplifier

Three non-idealities of the OTA contribute the pulse width error: input offset, limited bandwidth, and output referred noise. Because there are process mismatches, the OTA would have an input offset. From (3.4), we include the effect of the input offset (V_{OFF}), then

$$t_{\Phi 1} G_m (V_{REF} + V_{OFF}) + \int_0^{t_{\Phi 2}} G_m (V_{IN}(t) + V_{OFF})\, dt - T_{PW} G_m (V_{REF} - V_{OFF}) = 0 \quad (3.6)$$

$$T_{PW} = \frac{V_{REF}-V_{OFF}}{V_{REF}} = t_{\Phi 1} + \frac{\int_0^{t_{\Phi 2}} V_{IN}(t)dt}{V_{REF}} + \frac{2V_{OFF}t_{\Phi 1}}{V_{REF}}. \quad (3.7)$$

As shown in (3.7), V_{OFF} occurs a gain error and offset that can be calibrated.

To analyze the effect of the limited bandwidth of the OTA, we added a first order low-pass filter after the ideal OTA. The step response of the first order low-pass filter can be expressed as A(1-exp(-t/τ)) where A is amplitude and τ is a time constant. At the beginning of the Φ1, the input voltage of the OTA is changed from 0 to V_{REF}. Therefore, the output current of the OTA is

$$I_{\Phi 1} = G_m \times V_{REF}(1 - e^{-\frac{t}{\tau}}). \quad (3.8)$$

Similarly,

$$I_{\Phi 2} = G_m[(V_{IN}(t_{\Phi 1}) - V_{REF})\left(1 - e^{-\frac{t}{\tau}}\right) + V_{IN}(t) - V_{IN}(t_{\Phi 1}) + V_{REF}] \quad (3.9)$$

$$I_{\Phi 3} = G_m[(-V_{REF} - V_{IN}(t_{\Phi 2}))(1 - e^{-\frac{t}{\tau}}) + V_{IN}(t_{\Phi 2})]. \quad (3.10)$$

because the difference of charges stored in the sampling capacitors from the beginning of Φ1 and the end point is 0,

$$\int_0^{t_{\Phi 1}} I_{\Phi 1}\ dt + \int_0^{t_{\Phi 2}} I_{\Phi 2}\ dt + \int_0^{T_{PW}} I_{\Phi 3}\ dt = 0. \quad (3.11)$$

If we ignore the clock jitter ($|t_{\Phi 1}|=|t_{\Phi 2}|$), then

$$V_{REF}\left(\mathrm{T_{PW}} + \tau e^{-\frac{T_{PW}}{\tau}}\right) + V_{IN}(t_{\Phi 2})\tau e^{-\frac{T_{PW}}{\tau}} = \int_0^{t_{\Phi 2}} V_{IN}\,(t)\ dt$$

$$+\tau\left(V_{REF}+V_{IN}(t_{\Phi 2})\right)+t_{\Phi 1}V_{REF}-V_{IN}(t_{\Phi 1})(\tau-\tau e^{-\frac{t_{\Phi 1}}{\tau}}) \quad (3.12)$$

Assume $\exp(-T_{PW}/\tau)<<1/2^n$ and $\exp(-t_{\Phi 1}/\tau)<<1/2^n$ (n = resolution of the PWM), then

$$T_{PW}=\frac{\int_0^{t_{\Phi 2}}V_{IN}(t)\,dt}{V_{REF}}+t_{\Phi 1}+\tau+\tau\frac{V_{IN}(t_{\Phi 2})-V_{IN}(t_{\Phi 1})}{V_{REF}}. \quad (3.13)$$

$$\Delta T_{PW,OTABW}=\tau+\tau\frac{V_{IN}(t_{\Phi 2})-V_{IN}(t_{\Phi 1})}{V_{REF}}. \quad (3.14)$$

The output referred noise of the OTA distorts the sampling capacitor voltage. The PWM signal is generated at Φ3 (see Fig. 3.3) where the sampling capacitor voltage changes with the slope of $-G_mV_{REF}/C$. Therefore,

$$\Delta T_{PW,OTA}=\frac{CV_{noise,OTA}}{G_mV_{REF}}. \quad (3.15)$$

The noise of the OTA is generally composed of two parts: flicker noise ($V_{f,OTA}$) and thermal noise. Because the flicker noise is inversely proportional to the frequency and device size, the flicker noise is relatively smaller than thermal noise in the large device (both of width and length) with wide bandwidth. In thermal noise, because the capacitor is loaded by OTA, thermal noise is expressed by $\sqrt{(kT/C)}$, where k is Boltzmann constant, T is absolute temperature, C is the capacitance of sampling capacitor. Therefore, larger sampling capacitance helps to reduce the noise.

3.5.2 Comparator

As explained in section 3.2.A, the delay of the comparator can be compensated. On the other hand, the comparator input referred noise contributes noise on the sampling capacitor voltage. Therefore, the comparator input referred noise also follows (3.15).

Because the noise of the comparator and OTA are uncorrelated, the overall noise on the sampling capacitor is

$$\Delta T_{PW,C} = \frac{C\sqrt{V_{noise,OTA}^2+V_{noise,comp}^2}}{G_m V_{REF}}. \tag{3.16}$$

3.5.3 Clock jitter

Because the control signal of the PWM is generated based on the clock signal, the clock jitter of the input clock signal is directly related to the PWM performance. We evaluate the effect of the clock jitter in each phase. From (3.5), effect of in the clock jitter at the beginning of Φ1 (t_{j1}) is

$$(t_{\Phi 1}+t_{j1})G_m V_{REF} + \int_0^{t_{\Phi 2}} G_m V_{IN}(t)\,dt - T_{PW} G_m V_{REF} = 0 \tag{3.17}$$

$$T_{PW} = t_{\Phi 1} + t_{j1} + \frac{\int_0^{t_{\Phi 2}} V_{IN}(t)\,dt}{V_{REF}} \tag{3.18}$$

$$\Delta T_{PW,\Phi 1} = t_{j1.} \tag{3.19}$$

Considering the jitter at the beginning of Φ2 (t_{j2}), the equation is

$$G_m[(t_{\Phi 1}-t_{j2})V_{REF} + \int_{-t_{j2}}^{t_{\Phi 2}} V_{IN}(t)\,dt - T_{PW} V_{REF}] = 0 \tag{3.20}$$

$$T_{PW} = t_{\Phi 1} - t_{j2} + \frac{\int_0^{t_{\Phi 2}} V_{IN}(t)\,dt + \int_{-t_{j\,2}}^{0} V_{IN}(t)\,dt}{V_{REF}} \tag{3.21}$$

$$\Delta T_{PW,\Phi 2} = -t_{j2} + \frac{\int_{-t_{j\,2}}^{0} V_{IN}(t)\,dt}{V_{REF}} \tag{3.22}$$

Similar to (3.16), the effect of jitter at the beginning of Φ3 (t_{j3}) is

$$T_{PW} = t_{\Phi 1} + \frac{\int_0^{t_{\Phi 2}} V_{IN}(t)\,dt + \int_{t_{\Phi 2}}^{t_{\Phi 2}+t_{j3}} V_{IN}(t)\,dt}{V_{REF}} \quad (3.23)$$

$$\Delta T_{PW,\Phi 3} = \frac{\int_{t_{\Phi 2}}^{t_{\Phi 2}+t_{j3}} V_{IN}(t)\,dt}{V_{REF}}. \quad (3.24)$$

Let assume V_{IN} has uniform distribution from $-V_{REF}$ to V_{REF}, then the root-mean-square (RMS) of V_{IN} is $V_{REF}/\sqrt{3}$. Assume all of the clock jitters are the same amount of time (t_j) but uncorrelated, then

$$\Delta T_{PW,CLK}^2 = \Delta T_{PW,\Phi 1}^2 + \Delta T_{PW,\Phi 2}^2 + \Delta T_{PW,\Phi 3}^2 = t_j^2 + \frac{\left(1-\sqrt{3}\right)^2}{3}\frac{1}{3}t_j^2 \cong 1.51 \quad (3.25)$$

If we assume V_{IN} is a sine wave with an amplitude of V_{REF}, then the root-mean-square (RMS) of V_{IN} is $V_{REF}/\sqrt{2}$. Then,

$$\Delta T_{PW,CLK}^2 = t_j^2 + \frac{\left(1-\sqrt{2}\right)^2}{2}t_j^2 + \frac{1}{2}t_j^2 \cong 1.59t_j^2. \quad (3.26)$$

To reduce the noise caused by clock jitter, since the period of a clock is more accurate than the duty of a clock, we apply twice higher frequency clock (40 MHz) and divide it by half (20 MHz).

3.5.4 Receiver

Although the lower SNR increases error rate, the SNR of the Rx is not directly related to the resolution of the IR-PWM [73]. However, because of the noise from outside and aliasing of nearby impulse, the shape of the received impulse varies in time. To recover the data accurately, we need to measure the exact time difference between the rising and falling edge of the PWM signal. Because, in the Rx ASIC, the inverter follows the envelope

detector, the switching point where the envelope detector output passes the switching voltage of the inverter is regarded as either rising or falling edge of the PWM signal. However, the actual timing of the edges is more related to the time when the Rx starts to receive power. Therefore, the difference between the time and the switching point is considered as an error. The IR-PWM has two kinds of the impulses which are corresponding to the beginning (t_r) and end (t_f) of the PWM signal respectively, if t_r and t_f are the same, errors are canceled. However, the variation of t_r and t_f considered as a pulse width error, and the total receiver noise is

$$\Delta T_{PW,Rx} = \sqrt{\Delta t_r^2 + \Delta t_f^2}. \quad (27)$$

3.5.5 Design parameters

As mentioned in section 3.2, the application requires 35 dB SNR, and, considering the target dynamic range of pulse width (44 ns), total RMS pulse width error should be less than 782 ps. Since low clock jitter is hard to achieve in the specific application [59], we assigned a quarter of maximum pulse width error (195.5 ps) for the error occurred from the clock jitter. From (3.26), the required clock jitter was 155 ps.

To achieve more than the 8-bit resolution from the linearity measurement (INL and DNL), the PWM's input dynamic range was limited to -300 mV ~ 300 mV, and the maximum sampling capacitor voltage variation (V_{cap+} and V_{cap-} in Fig. 3.4) was limited up to 200 mV. To fit the input dynamic range into pulse width dynamic range, we set the reference voltage at 350 mV. Since, based on the simulation results, the noise of OTA and comparator could be easily minimized, we set the noise level less than 195 μV ($1/2^{10}$ of

200 mV) to make the noise from the OTA and comparator negligible. To make √kT/C noise of the sampling capacitors less than 195 μV, the capacitance of 110 fF is required. However, because the comparator has an intentional mismatch on the input pair to generates offset (explained in section 3.2.2), we used a larger capacitor (3.2 pF) to minimize the capacitance mismatch smaller than 0.4 % of the overall sampling capacitance.

The constant pulse width offset could be easily subtracted, but it limits the dynamic range of PWM signal. From (3.14), the bandwidth of OTA was designed to be 250 MHz to make the offset and error less than 1 ns and 85 ps ($1/2^9$ of the maximum pulse width) with 1 MHz sinusoidal wave. To avoid that the switches (Φ1, Φ2, and Φ3 in Fig.3a) limit the bandwidth of OTA, the size of them were designed to have -3 dB bandwidth of 2.5 GHz with the input capacitance of the OTA.

3.6 Measurement Results

An IR-PWM ASIC prototype was fabricated in the TowerJazz 0.18-μm power management CMOS process, occupying 0.18 mm^2 (active area) (Fig. 3.6). The IR-PWM transmitter consumes 2.7 mW and 1.24 mW at 1.8 V respectively. Energy consumption of IR-PWM was 197 pJ/sample which means 28.1 pJ/bit considering a 7-bit resolution of the PWM. The energy consumption of IR transmitter without the PWM was 8.86 pJ/bit. In the design phase, we assumed 3 ns delay between consecutive impulses is enough to avoid inter-symbol interference (ISI). From the measurement results, however, if two IR-PWM pulses are closer than 7.5 ns, becomes higher because of limited bandwidth of wireless link. Therefore, we adjusted the reference voltage from 350 mV to 450 mV to limit the output dynamic range. The sampling rate of the IR-PWM was 10 MS/s, but two IR-PWM shared

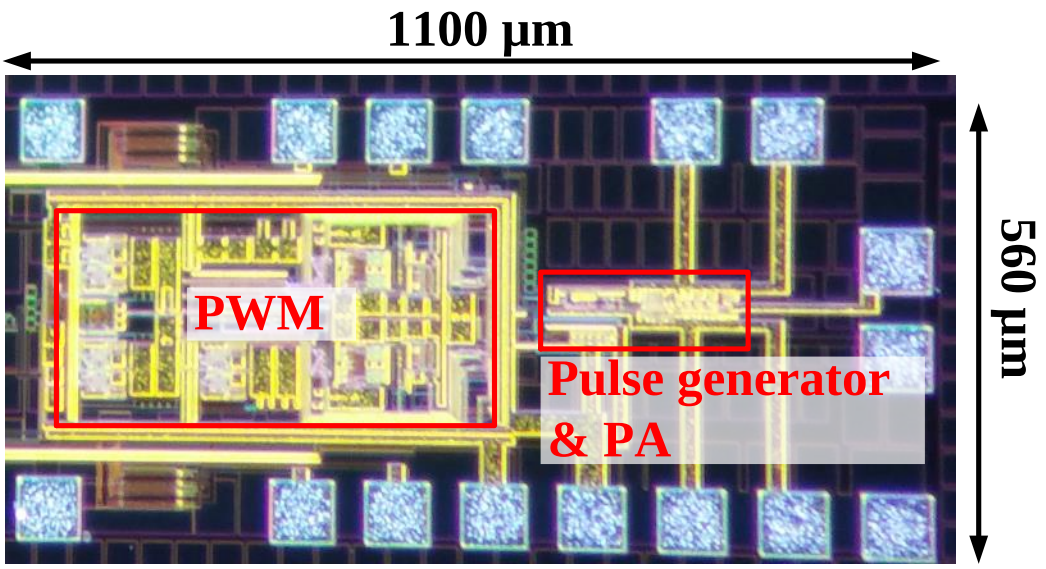


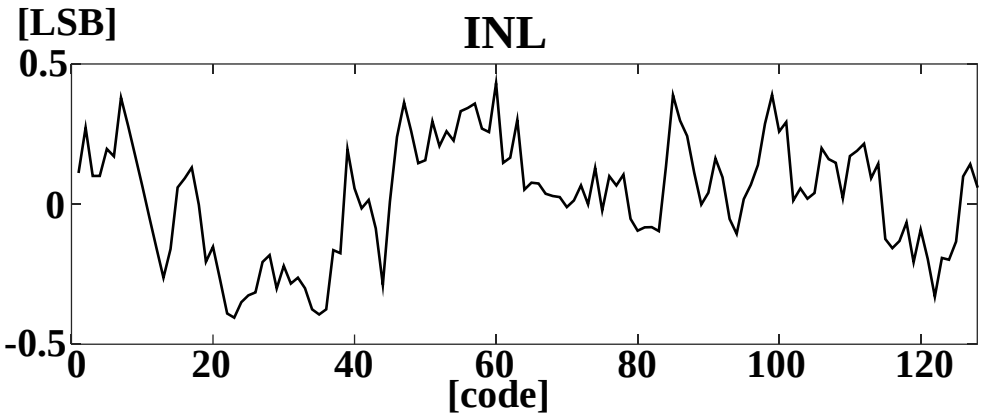
Figure 3.6. Die photo of IR-PWM transmitter.

Table 3.1 - Benchmarking low-power wireless transmitters

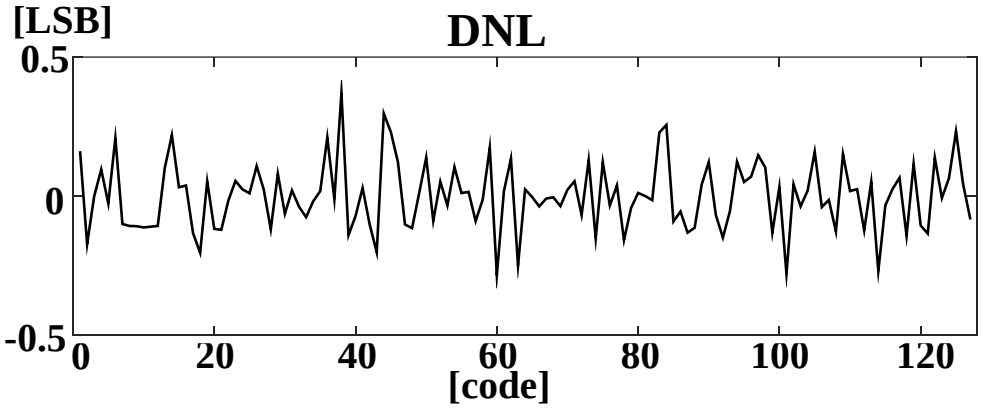
Transmitter	[75]	[76]	[77]	[78]	This work
Modulation	OOK-UWB	OOK-UWB	BPSK-BCC	OOK / FSK	IR-PWM
Technology (nm)	180	90	65	180	180 PM*
Frequency (GHz)	3-5	3-5	0.14 - 0.18	2.4	0.8-1.5
Energy/bit (pJ/bit)	350	30	32.5	38	8.86 / 28.1***
Active area (mm^2)	12**	0.061	5.76**	0.035	0.18
Data rate (Mbps)	10	67	5 - 80	5	2 × 70
Tx Range (cm)	20	50-400	-	-	15

*PM= Power management CMOS process (High voltage CMOS available)
**Include PADs area.
*** Transmitter only/The entire IR-PWM

the data communication channel, 2 × 10 MS/s sampling rate was achieved. Table 3.1 summarizes the specifications of wireless communication part and compared to existing



(a)



(b)

Figure 3.7. Measurement results for 7-bit (a) INL and (b) DNL.

state-of-the-art works.

Since the PWM does not directly generate the digital code, the resolution is not defined by the PWM itself but the TDC also contributes its resolution. We recorded the PWM signal with the oscilloscope with a 50-ps sampling rate which is the 9-bit time resolution in the PWM signal dynamic range of 46 ns. In [74], the resolution of the PWM was defined by INL and DNL. Based on the definition, the resolution of the proposed PWM was 7-bit where INL and DNL are less than +/- 0.5 LSB (Fig. 3.7). The resolution was less than what we expected in simulation results (8-bit), and 10 % less resistance value on

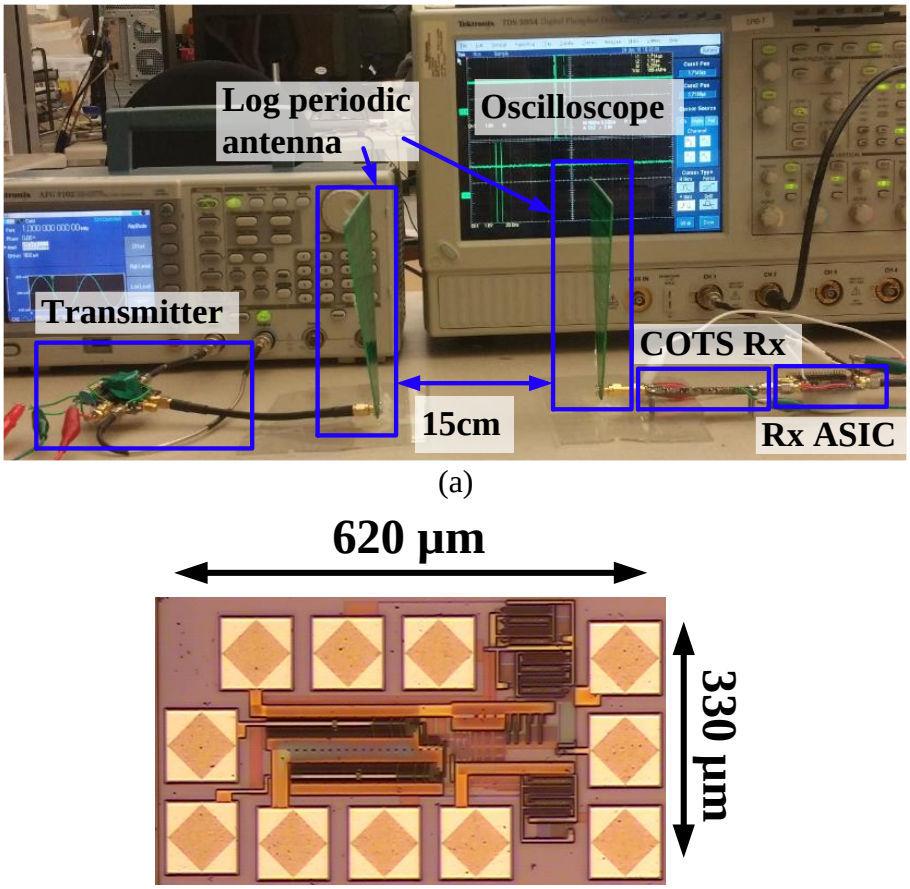


Figure 3.8. (a) Measurement setup of IR-PWM transceiver and (b) die photo of the Rx ASIC.

degeneration resistor of the OTA (Fig. 3.5b) could limit the linearity by 7-bit.

Fig. 3.8a shows the IR-PWM measurement setup. Because of the limited speed of the process and the IR-PWM Tx transmitted a single impulse, a low-frequency impulse with a spectrum of 0.6 ~ 1.5 GHz used in this ASIC to transmit more power. To receive the low-frequency signal, we used log periodic antennas (WA5VJB, Kent Electronics, Sugar Land, TX) which cover 0.85 ~ 6.5 GHz. Because the focus of this work is proving the concept of the IR-PWM, Rx and Tx antennas were placed 15 cm apart to achieve high enough SNR that guarantees the negligible error rate. The Rx ASIC in the receiver was fabricated in TSMC 0.35-µm standard CMOS process occupying 0.2 mm^2 (Fig. 3.8b).

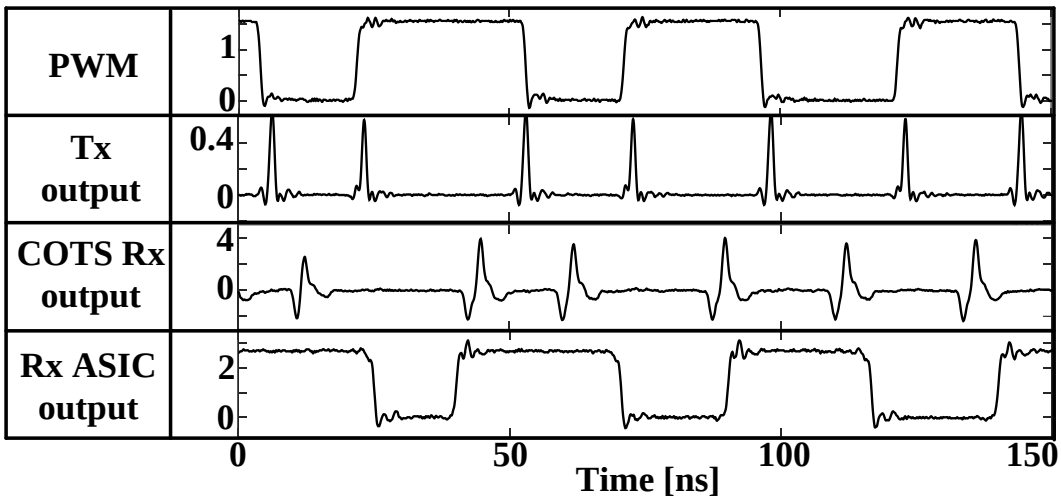


Figure 3.9. Measured signals from Tx PWM, Tx output, COTS Rx output, and recovered Rx ASIC output PWM with 30 ns latency.

To measure the effective number of bits (ENOB), we conducted a single-tone test with a 1-MHz sinusoidal wave. Since the oscilloscope has memory limitation and PWM signal requires high sampling rate, we measured signals for 20 μs. We decoded PWM data from the recorded Tx output, the COTS Rx output, and the Rx ASIC output, and plotted in Fig. 3.9. To prevent the distortion of the signal, we separately measured each output with 50 Ω termination without following stages. In addition, because each stage had a certain level of delay, the edges of each output were not synchronized. Based on the decoded data, we measured SNR, spurious-free dynamic range (SFDR), and signal-to-noise and distortion ratio (SINAD) (Fig. 3.10). SINAD of the transmitter output and the recovered PWM signal are 39.7 dB and 36.8 dB respectively, and the corresponding ENOB of them were 6.3 and 5.8 bits respectively. Table 3.2 summarizes the specifications and compared to other types of ADC topologies.

To analyze noise contribution by following the discussion in section 3.3, we measured the clock jitter, the input signal noise, and the Rx signal. A function generator

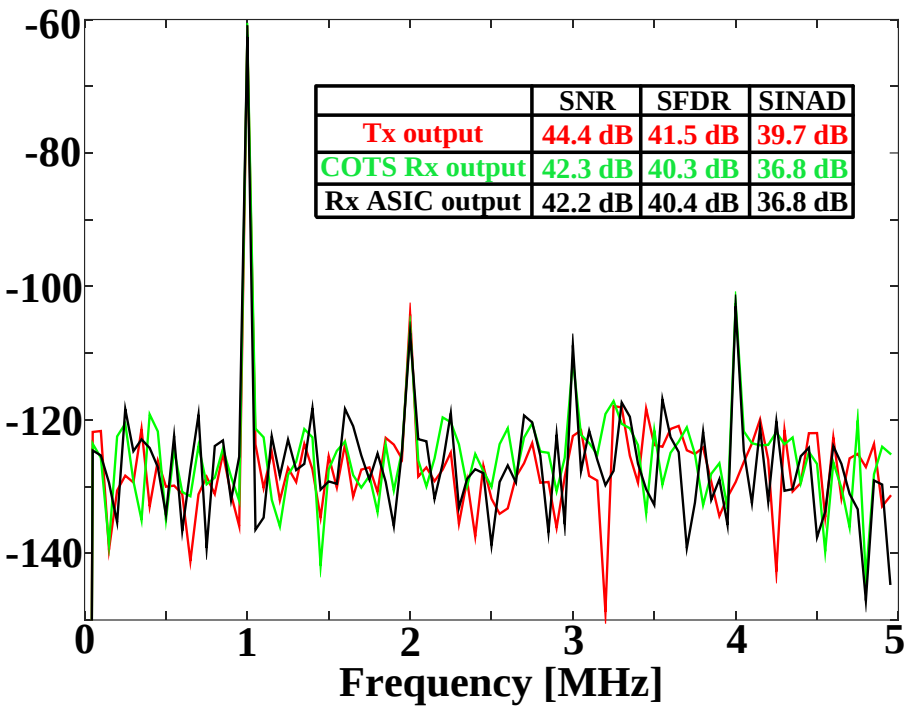


Figure 3.10. Spectrum of decoded Tx output, COTS Rx output, and Rx ASIC output.

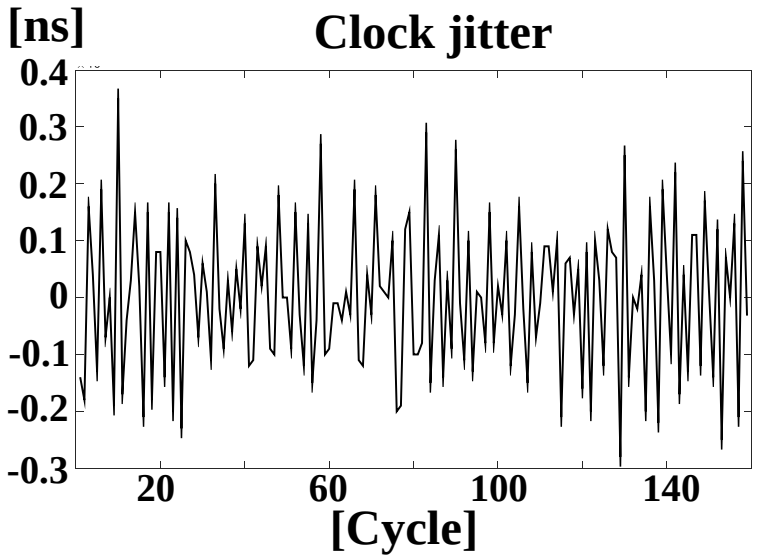


Figure 3.11. Measured clock jitter output.

(AFG 3102, Tekronix) applied a 40 MHz square wave as a clock signal and the measured jitter of it is depicted in Fig. 3.11. The RMS of jitter was 126.42 ps. Since we applied a sinusoidal wave as an input, corresponding PWM noise ($\Delta T_{PW,CLK}$) was 159.41 ps by following (3.26). Since the OTA and comparator were not possible to access, the noise

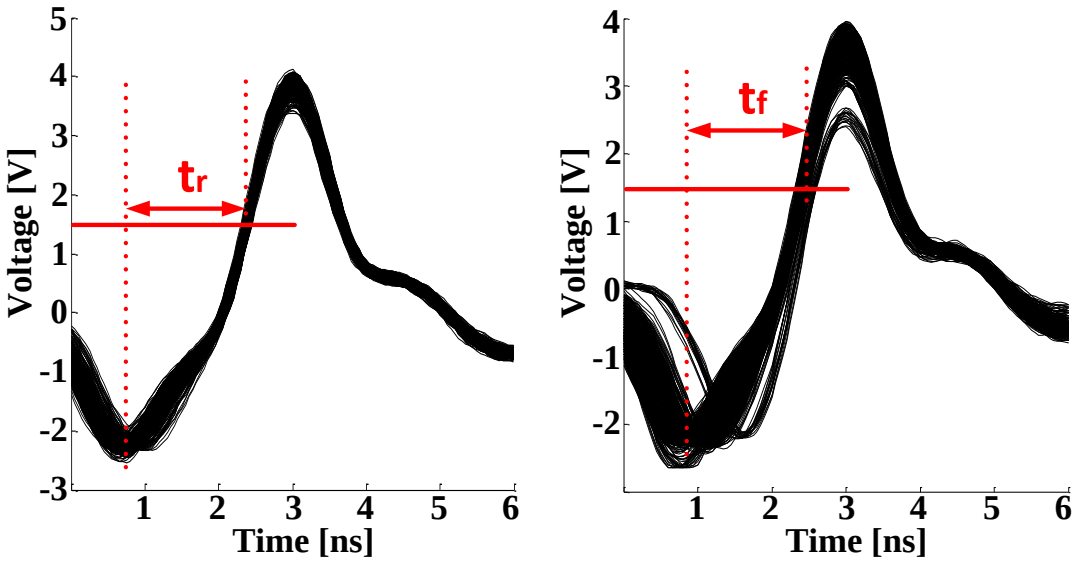
Table3.2 - Benchmarking ADC part

ADC	[69]	[64]	[79]	[80]	This work
Type	PWM	SAR	SAR	SAR	PWM
Technology (nm)	350	130	130	65	180 (PM)*
Sampling rate (MS/s)	8 × 0.031	50	30	50	2 × 10
Resolution	8	10	14	13	7
Power (mW)	-	0.826	2.54	1	2.7**
Active area (mm^2)	0.29	0.052	0.24	0.054	0.18

*PM= Power management CMOS process (High voltage CMOS available)
** Include Tx power consumption.

measurement of them was replaced with simulation results. In the simulation results, the input referred noise of the comparator was 141 nV and the output referred noise of the OTA including the noise of sampling capacitors was 40.5 μV. The simulation results also showed that the G_m of the OTA was 70 μA/V with -3 dB bandwidth of 250 MHz. From (3.16), the $\Delta T_{PW,C}$ was 7.7 ps. Because τ of the OTA is 0.636 ns and the minimum T_{PW} is 7.5 ns, the assumption for (3.14) is valid for the entire input dynamic range. From (3.14), the OTA induced an offset of ~0.64 ns and, considering 1 MHz sinusoidal wave, the RMS pulse width error of 47.05 ps.

As shown in Fig. 3.12, the Rx output have a negative peak followed by a positive peak. The negative peak represented the starting point of receiving signal and it implied the time when a Tx impulse was transmitted. However, the Rx AISC recognize the point where receiver signal passes the switching voltage of the inverter as an edge of PWM signal. Therefore, to measure the distortion from the wireless link, we measured the time



(a) (b)

Figure 3.12. Measured switching time variations of the impulses that correspond to (a) rising and (b) falling edges of the PWM signal.

difference between the first negative peak of the COTS Rx output and the time when the COTS Rx output pass the switching voltage (t_{diff}). Because, in the PWM, the receiver pulses can be divided into two types, rising and falling edge of PWM signal, we measured the t_{diff} and divided it into t_r and t_f in Fig. 3.12. If the t_r and t_f are constant in all the pulses, it can be canceled as an offset. Therefore, we calculated the variation of t_r and t_f that contributed on the distortion. The measured RMS of the Δt_r and Δt_f were 75.25 ps and 88.17 ps respectively. The input sinusoidal wave was also generated from the same function generator and the SNR of the input signal was 55.3 dB.

Based on the measured values, the equivalent SNR and equivalent number of bit (NOB) are calculated from the equation

$$Equivalent\ SNR = \frac{T_{PW.max}}{\Delta T_{PW}} \tag{3.28}$$

Table 3.3 - Noise contribution of different blocks

	Equivalent SNR	Equivalent NOB
Input signal	55.3 dB	8.89 bit
OTA and comparator noise ($\Delta T_{PW,C}$)	72.73 dB*	11.78 bit*
OTA bandwidth ($\Delta T_{PW,OTABW}$)	57 dB*	9.18 bit*
Input clock ($\Delta T_{PW,CLK}$)	46.83 dB	7.49 bit
Tx Total	41.14 – 45.32 dB	6.54 - 7.24 bit
Receiver($\Delta T_{PW,Rx}$)	49.17 dB	7.87 bit
Total	38.24 – 43.82 dB	6.06 - 6.99 bit

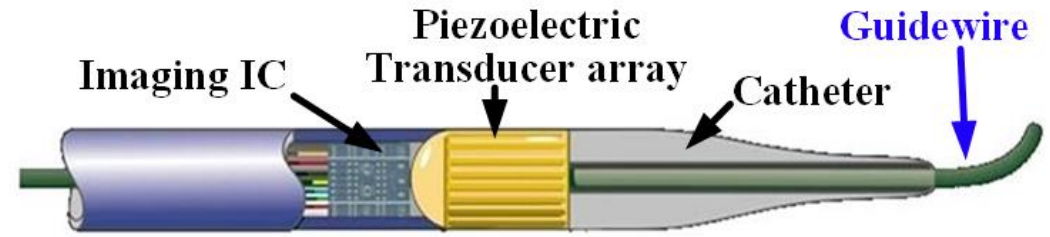
*Only provided simulation results on noise of OTA and comparator.

$$Equivalent\ NOB = \frac{Equivalent\ SNR - 1.76}{6.02}. \tag{3.29}$$

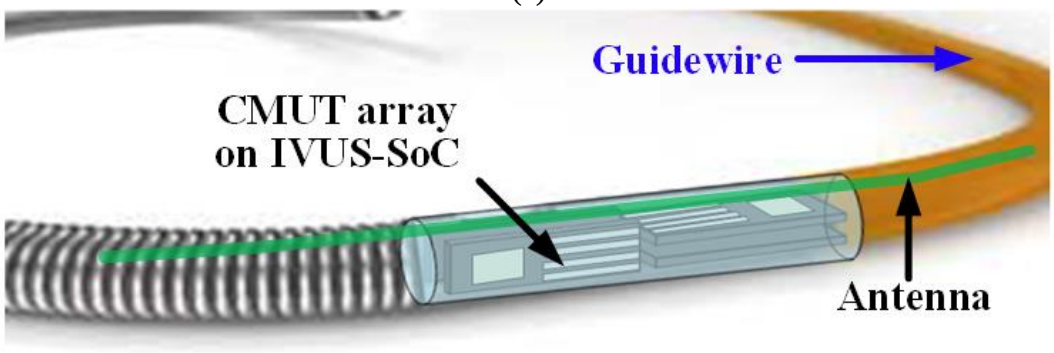
If we assume all the noise sources are uncorrelated, expected equivalent SNR of the Tx output from the noise source was 45.32 dB. However, if they are correlated each other, then the equivalent SNR could drop to 41.14 dB. To simplify the analysis, we ignore the relationship between each noise source. Although the effect of the other noise source is not significant, considering the resolution, the relation between the noise sources is not negligible. Therefore, the measured SNR at Tx output (44.4 dB) was located between the best and the worst case. Similarly, total equivalent SNR including Tx and Rx noise (42.2 dB) was located between the best (43.82 dB) and the worst case (38.24 dB). As we shown in Fig. 3.7, the IR-PWM had 7-bit resolution and it contributed the harmonic distortion. Therefore, the measured ENOB of the IR-PWM was 5.8 bit is lower than the equivalent NOBs from the noise source (6.1 – 7 bit). Table 3.3 summarized the noise contributions.

CHAPTER 4. RX-ONLY WIRELESS READ-OUT SYSTEM FOR GUIDEWIRE IVUS SYSTEM

As mentioned in chapter 1, because intravascular ultrasound (IVUS) provides real-time and high-resolution images of the arteries with negligible side effects, it has been a common imaging modality for cardio-vascular interventions.



(a)



(b)

Figure 4.1. (a) Conceptual rendering of the current piezoelectric transducer array based IVUS imaging system [58]; (b) rendering of the proposed CMUT based guidewire IVUS, superimposed over a St Jude Certus guidewire [81].

In contrast, flexible guidewires with diameters ranging from 0.36 to 0.89 mm (1.1F-2.67F) are commonly used in coronary interventions along with balloon and stent catheters, as well as IVUS catheters, which are threaded over these guidewires (Fig. 4.1a) [82]. Integrating IVUS imaging directly on the guidewires would lead to a paradigm shift, i.e. IVUS can be used “during” interventions without an extra catheter exchange. Moreover,

the IVUS can reach narrow arteries where most of the lesions are occurring. This potential has been recognized and envisioned for two decades and guidewire IVUS systems based on rotating single transducer have been proposed [83], [84]. These early approaches, however, were not pursued most probably because of difficulties in mechanical implementation. In the meantime, non-rotating solid-state IVUS arrays [85], and integration of ultrasonic transducer arrays and their interface electronics, such as CMUT-on-CMOS technology, have been realized [67], and in fact pressure sensors for fractional flow reserve (FFR) and Doppler flow sensors have been successfully integrated on guidewires [86]. These advances indicate the need and potential for guidewire IVUS based on phased arrays. Fig. 1b presents a conceptual diagram of the proposed guidewire IVUS imaging system which depicts 4 CMUT-on- CMOS phased arrays, each imaging a separate sector of the arterial wall, to form a complete cross-sectional image without rotation. In the final system, 3D-IC technology will be adopted in addition to CMUT-on-CMOS to accommodate all the necessary SoC components within the guidewire.

Several aspects of the IVUS systems need to be considered to specify the design targets on the SoC and the CMUT array. To achieve sufficient resolution similar to the conventional phased array IVUS catheters, which operate in the 20 MHz range, the smaller CMUT array on the 0.36 to 0.89 mm guidewire should operate in the 40 MHz frequency range. Because the axial (R_A) and lateral (R_L) resolutions of the ultrasound image are defined by,

$$R_A = \frac{c}{2 \times bandwidth} \tag{4.1}$$

$$R_L = \frac{Depth \times \lambda}{Array\ size} \tag{4.2}$$

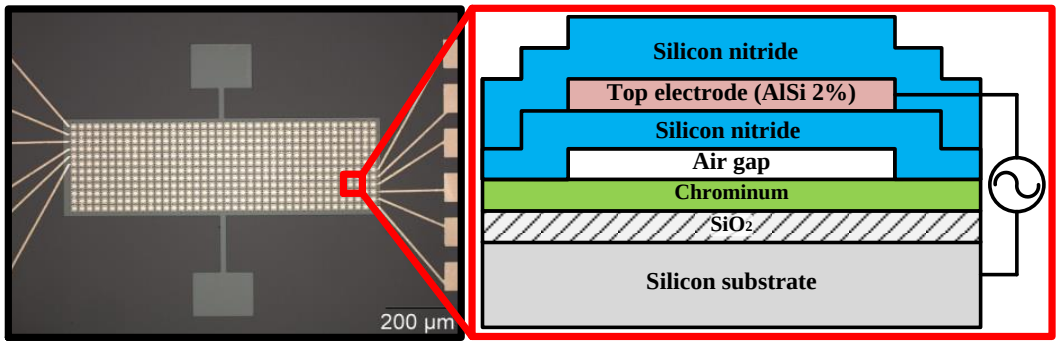
where c =1540 m/s is the speed of sound in tissue medium and λ = 37 μm is the ultrasound wavelength [87]. Furthermore, the number and cross-sectional area used for electrical wires need to be reduced as much as possible so that the impact on the mechanical properties, particularly flexibility, of the guidewire is minimized. Considering the average length of the guidewire, reaching ~2.6 m, the parasitic resistance of the thin and highly flexible wires would be considerable and not only limit the analog signal bandwidth for data readout but also increase their vulnerability to noise and interference. Therefore, either digitized or pseudo-digital raw data transfer across the guidewire should be considered. Since the target guidewire IVUS operates around 40 MHz with a bandwidth of 10 MHz, digitizing raw data should be performed at least at 90 MS/s, generating data rates close to 1 Gb/s. In addition to such a high sampling rate, an even higher clock frequency is needed, leading to more power consumption and more complexity in the interface SoC. On the other hand, since the system will be placed inside arteries, where blood perfusion helps with heat dissipation to a certain extent, power consumption can be up to 100 mW [88].

Given the above design targets, we have implemented a proof-of-concept IVUS imaging SoC prototype to explore the possibility of a guidewire IVUS that significantly reduces the number of interconnects, down to only two. The system uses minimum bandwidth required by quadrature sampling, where the received echo signal from the CMUT transducer is down- converted to baseband to decrease the required sampling rate by a factor of four [89] and employs analog to time conversion (ATC) technique to convert the raw data to a pseudo-digital pulse width modulated (PWM) signal [69], which is robust against noise while requiring much lower clock rate compared to a traditional ADC solution.

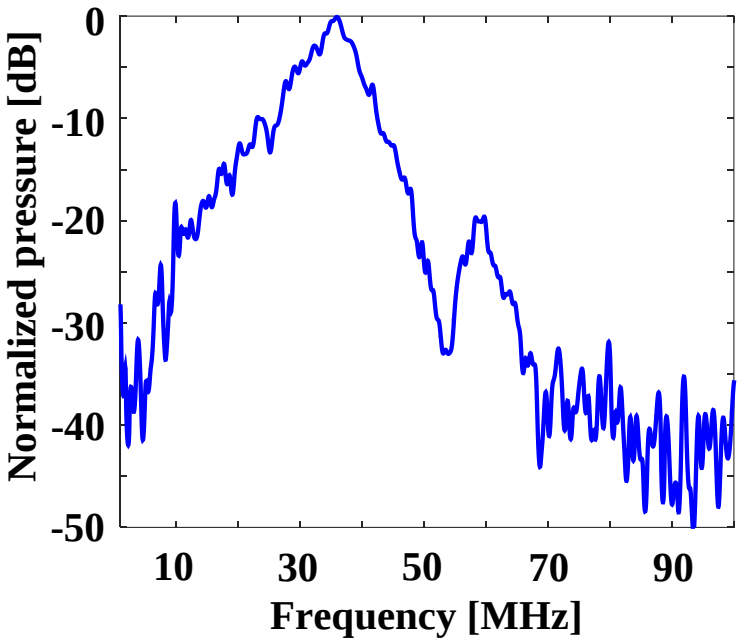
To reduce the number of wires for data transmission to two, we implemented an impulse radio ultra-wideband (IR-UWB) transmitter (IR-Tx) that is combined with our PWM raw data in a new approach to reduce power consumption on the RF data Tx side [66]. To reduce the SoC power consumption and system complexity, we adopted the synthetic-aperture imaging method that uses only one pair of transmitting (U-Tx) and receiving (U-Rx) CMUT elements for each ultrasound firing event [90].

4.1 1-D CMUT array for IVUS imaging

The elevation width of the guidewire severely limits the aperture size of the imaging array. This requires designing high-frequency transducer arrays to meet the specified resolution, according to (4.1) and (4.2). We utilized a custom-designed large signal simulation tool, described in [91], to model and design the CMUT arrays that meet the 40 MHz center frequency and 10 MHz bandwidth specifications. Since simulating the whole CMUT array is computationally intensive, only an array of 15 × 15 membranes was modeled in these simulations. As shown in Fig. 4.2a, square shaped silicon nitride membranes, 20 μm × 20 μm in size and 2 μm in thickness, were suspended over a 30 nm vacuum gap to satisfy the desired operating spectrum. A second 200 nm thick silicon nitride layer was used as the dielectric isolation layer above the gap. The CMUT array was fabricated using a low-temperature CMOS-compatible micromachining process, described in [92]. To minimize the grating lobe effects in the image, we designed a 12-element 1-D array with a pitch of 25 μm (2/3×λ) which can fit in 300 μm width. Each CMUT array element is composed of 40 membranes in the azimuth direction along a length of 1 mm. We targeted 40 MHz center frequency with a bandwidth of 35 - 45 MHz, and the resulting CMUT array had a -3 dB bandwidth of about 40 MHz around a 37 MHz center frequency,



(a)



(b)

Figure 4.2. (a) Layout of the 1-D CMUT array with multiple membranes in each of the 12 CMUT elements, (b) Normalized CMUT pressure frequency response in the transmitter mode.

as shown in Fig. 4.2b. Therefore, it was suitable for our preliminary measurements.

4.2 System architecture of Rx-only wireless read-out system for IVUS imaging

Block diagram of the prototype guidewire IVUS interface SoC is shown in Fig. 4.3a. A complete IVUS front-end would consist of a U-Tx driver block with high voltage pulsers and transmit logic in addition to the U-Rx block [39]. The focus of this article is on the U-Rx side of the IVUS front-end because, first, designing the U-Rx block is relatively

more complex than the U-Tx block. Secondly, the Tx block requires high voltage transistors (> 60 V), which were not available in our 5 V standard CMOS process. The presented front-end SoC has all the U-Tx and U-Rx functionality except for the high voltage pulsers, which are implemented off-chip using commercially available off-the-shelf (COTS) components, but can be easily integrated with the rest of the SoC in an HV-CMOS process.

4.2.1 Overall system

The guidewire IVUS system is powered by a 10 MHz power carrier signal provided by an external power amplifier (PA) and delivered through a pair of thin (58 µm diameter, AWG 42.5) wires, 2.4 m in length, running over the guidewire which are the only electrical interconnects needed to operate the proposed system. An on-chip full-wave rectifier, similar to [93], generates 3.7 V DC voltage from the power carrier, which is regulated down to 3.3 V to supply the IVUS SoC. In order to use a standard CMOS process with COTS pulsers, the CMUT array is divided into two groups, 6 U-Tx and 6 U-Rx elements, which are interlaced. Although this arrangement results in undesired grating lobes, it was adequate for our preliminary imaging demonstration purpose.

As shown in Fig. 4.3a, the top electrodes of the Rx CMUT array are connected to an array of transimpedance amplifiers (TIA) to convert the CMUT output current into a voltage output. To reduce power consumption and system complexity, we utilized synthetic-aperture imaging method, in which only one U-Rx CMUT and its associated TIA are activated at any time. A control circuit that is run by a signal derived from the power carrier, selects each U-Tx-Rx pair at 25.6 µs intervals based on the anticipated round-trip

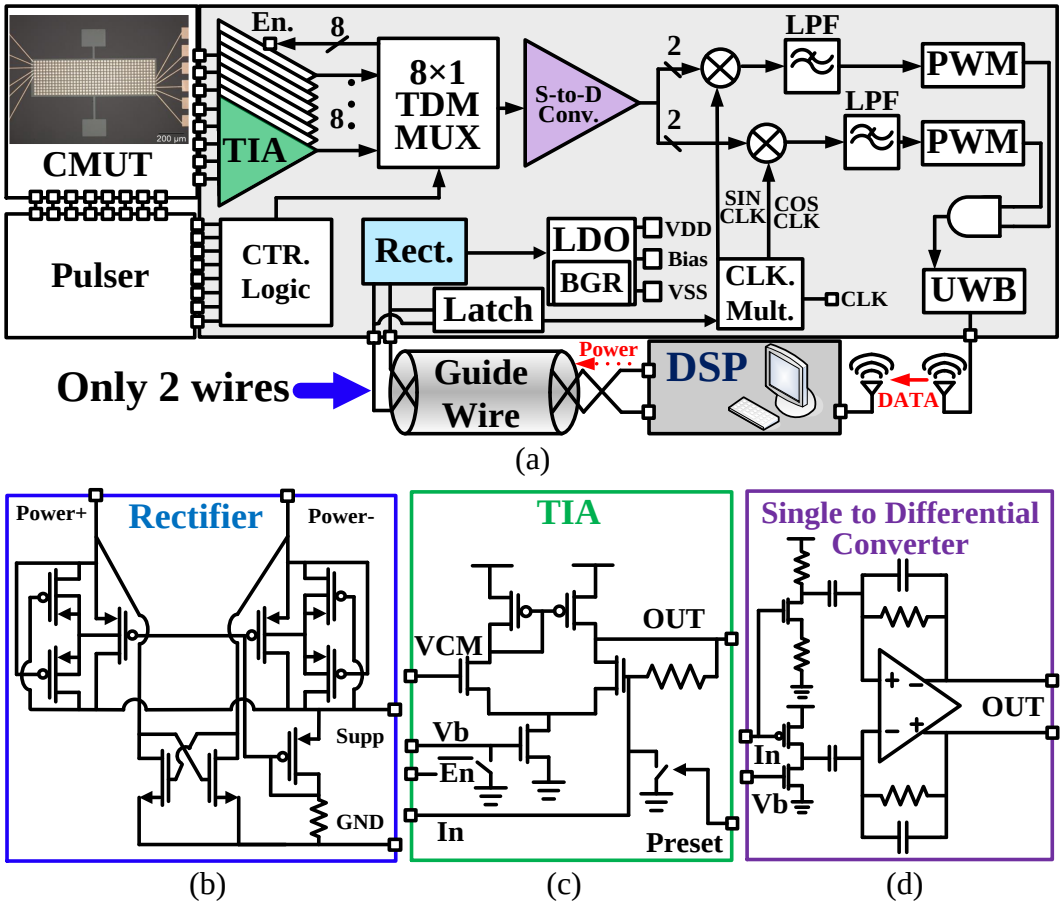


Figure 4.3. (a) Overall system block diagram of the IVUS imaging system, (b) schematic of full-wave passive rectifier, (c) transimpedance amplifier (TIA), and (d) a single-to-differential converter.

pulse-echo travel time from a target at 1 cm imaging depth [90]. To achieve better noise performance in the following stages, a single-to-differential converter was implemented to follow the TIA. Two identical direct down-conversion mixers constitute a quadrature sampler, while a local oscillator (LO) provides in-phase clock (I) and quadrature phase (Q) clock signals for each mixer. A clock multiplier was implemented to generate the I and Q clocks at 40 MHz from the 10 MHz power carrier since the CMUT center frequency is at 40 MHz. The 40 MHz clocks are also fed into a pair of pulse width modulators (PWM) that convert the down- converted I and Q signals to sequential PWM data at 10 MS/s. Finally, an AND-gate combines the two PWMs, in a way that the overall sampling rate

becomes 20 MS/s. An IR-UWB transmitter then generates sharp pulses at the rising and falling edges of each PWM data pulse, according to the method described in [66], and transmits them through a 0.4-1 GHz wideband antenna to outside of the body.

4.2.2 Power Management IC

A full-wave rectifier, shown in Fig. 4.3b, with a threshold- compensated diode-connected PMOS pair and a cross-coupled NMOS pair receives AC input voltage through the guidewire interconnects and generates an unregulated DC output voltage. This topology improves the power conversion efficiency (PCE) at 10 MHz and reduces the voltage drop across the rectifier while providing enough output power for the SoC. The rectifier supplies a 3.3 V regulator and a resistor-free bandgap reference (BGR) that occupies less area than a regular BGR [94].

4.2.3 Transimpedance amplifier

We used resistive feedback TIA, shown in Fig. 4.3c, for area efficiency, because the area of the required resistor in this process was smaller than that of a feedback capacitor [96]. The resistive feedback TIA was designed with a transimpedance gain and bandwidth of 28.5 kΩ and 20 MHz, respectively Although this bandwidth is smaller than the center frequency of the CMUT, these values have been optimized for the overall performance considering the power of the echo signal and the input referred noise with various TIA feedback resistor values, while limiting the power consumption to 6 mW.

Since the expected thermal mechanical noise of the targeted CMUT is larger than 2 pA/√Hz, we designed the TIA for an input-referred current noise of 1.5 pA/√Hz at 40 MHz. Moreover, the TIAs are turned off except for the TIA which is connected to the

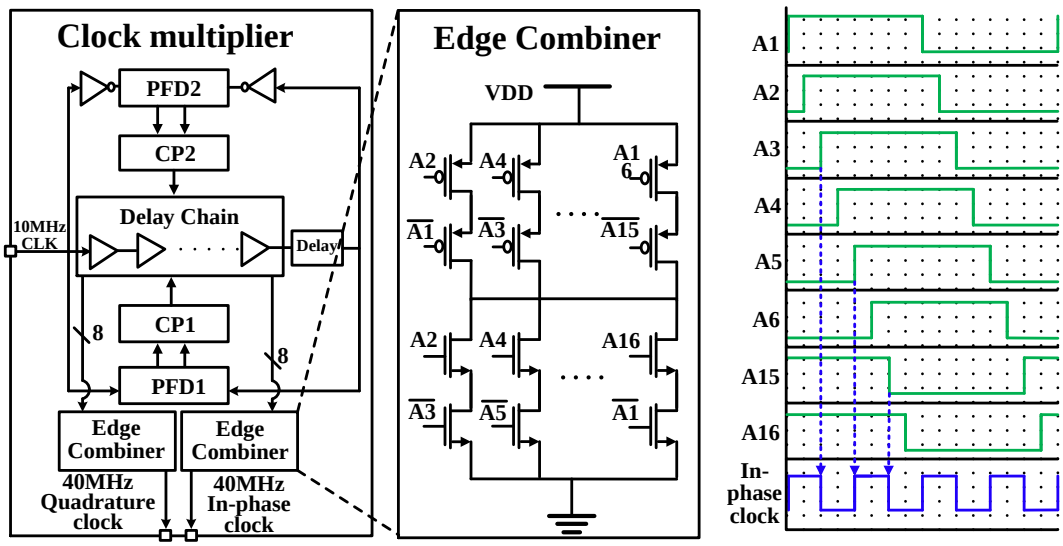
active Rx CMUT, to save power. We also implemented another switch (Preset) that significantly reduces the input impedance of the TIA during pulse transmission to prevent possible TIA saturation due to pulse feedthrough from the high voltage drive signals applied to the U-Tx CMUTs.

4.2.4 Single-to-differential converter

The IVUS SoC front-end utilizes direct down-conversion, in which the local oscillator (LO) leakage can affect the system performance. Therefore, a double-balanced mixer with differential input is preferred. As shown in Fig. 4.3d, a single-to-differential converter (STDC), consisting of a source follower, a source-degenerated common source, and a fully- differential amplifier, converts the single-ended TIA output to a differential signal. The source follower and CS amplifier are designed to improve positive and negative output balancing, and both have the large bandwidth (100 MHz) and low gain (-1.5 dB) to keep the phase constant at 0° and 180° in the echo signal frequency range (30~43 MHz). To reduce distortion, the overall bandwidth of the STDC is designed to be 25-90 MHz with a gain of 6 dB.

4.2.5 Clock multiplier

Fig. 4.4a shows the dual-loop delay-locked loop (DLL) that generates in-phase (I) and quadrature (Q) 40 MHz clocks from the 10 MHz power carrier. To achieve 7 effective number of bits (ENoB), the target resolution of this prototype, from the PWM, root-mean-square (RMS) of the clock jitter should be less than 1/256 of the maximum PWM pulse width, which is 50 ns at 20 MS/s, i.e. 99.9 ps [63]. This was the basis of the phase-frequency detector (PFD) and charge pump (CP) designs [97]. The DLL delay blocks are composed



(a) (b)

Figure 4.4. (a) Block diagram of a clock multiplier, and (b) the operation of an edge combiner.

of current-starved inverter chains, for which the operating range was selected based on the region where the current variation is less sensitive to the charge pump output voltage variations. Moreover, to compensate the effect of PFD dead time, we added another delay circuit after the delay chain. The delay chain generates 16 delayed signals, in which the rising and falling edges are combined, as shown in Fig. 4.4b, to generate the 40 MHz I and Q clock signals.

4.2.6 Quadrature sampler

Since double balanced mixers have good noise performance and high linearity, and double-balanced mixers have low LO leakage, we adopted a double-balanced mixer architecture, which operation and schematic are depicted in Fig. 4.5. The quadrature sampler converts 35 - 45 MHz band, which covers the spectrum of the received echo signal, to DC - 5 MHz baseband, such that the quadrature-sampler output actually shows the envelope of the echo signal. A fully-differential operational trans- conductance amplifier

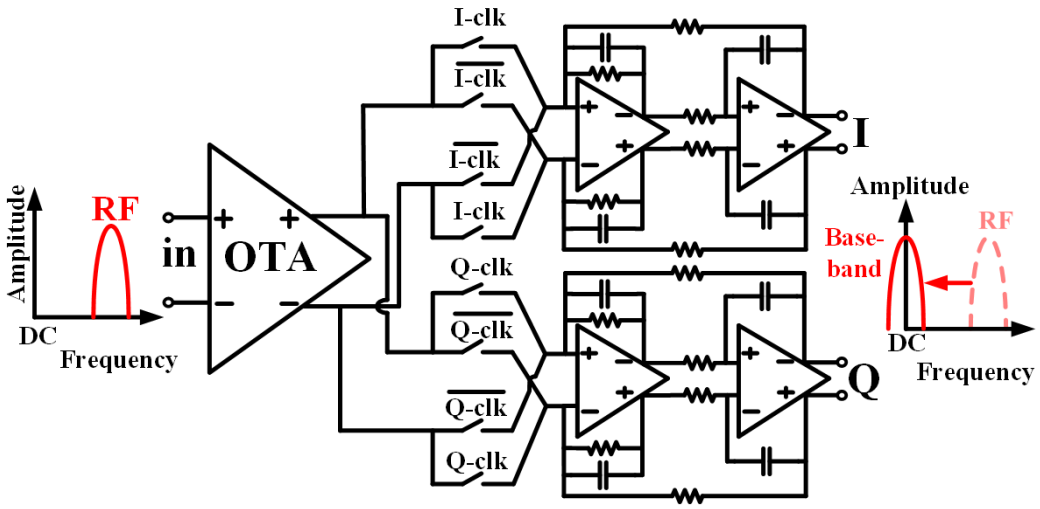
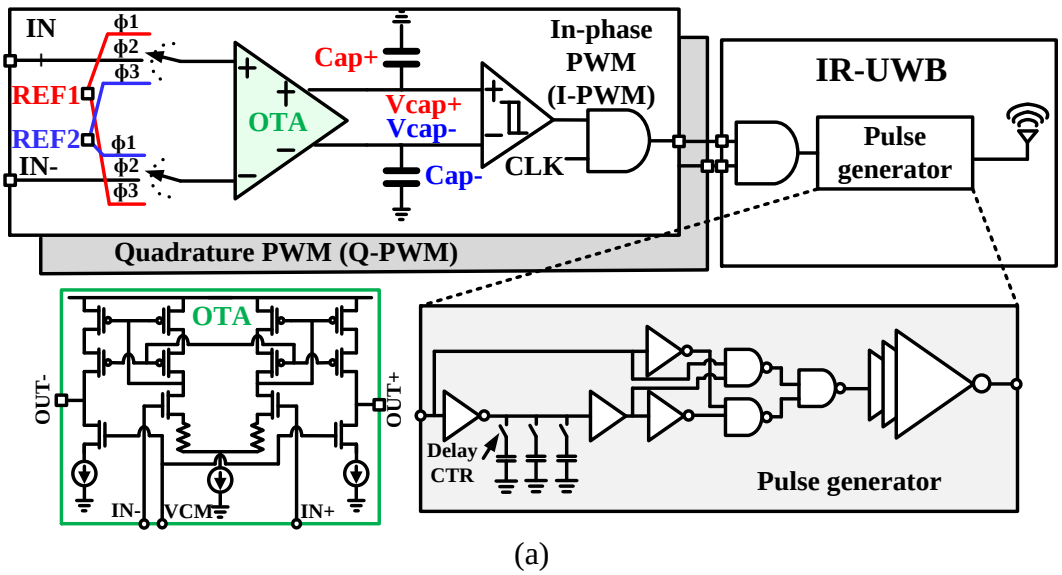


Figure 4.5. Operating waveforms and schematic diagram of the quadrature sampler. Two double-balanced mixers that share the same operational trans- conductance amplifier (OTA) are used in this quadrature sampler.

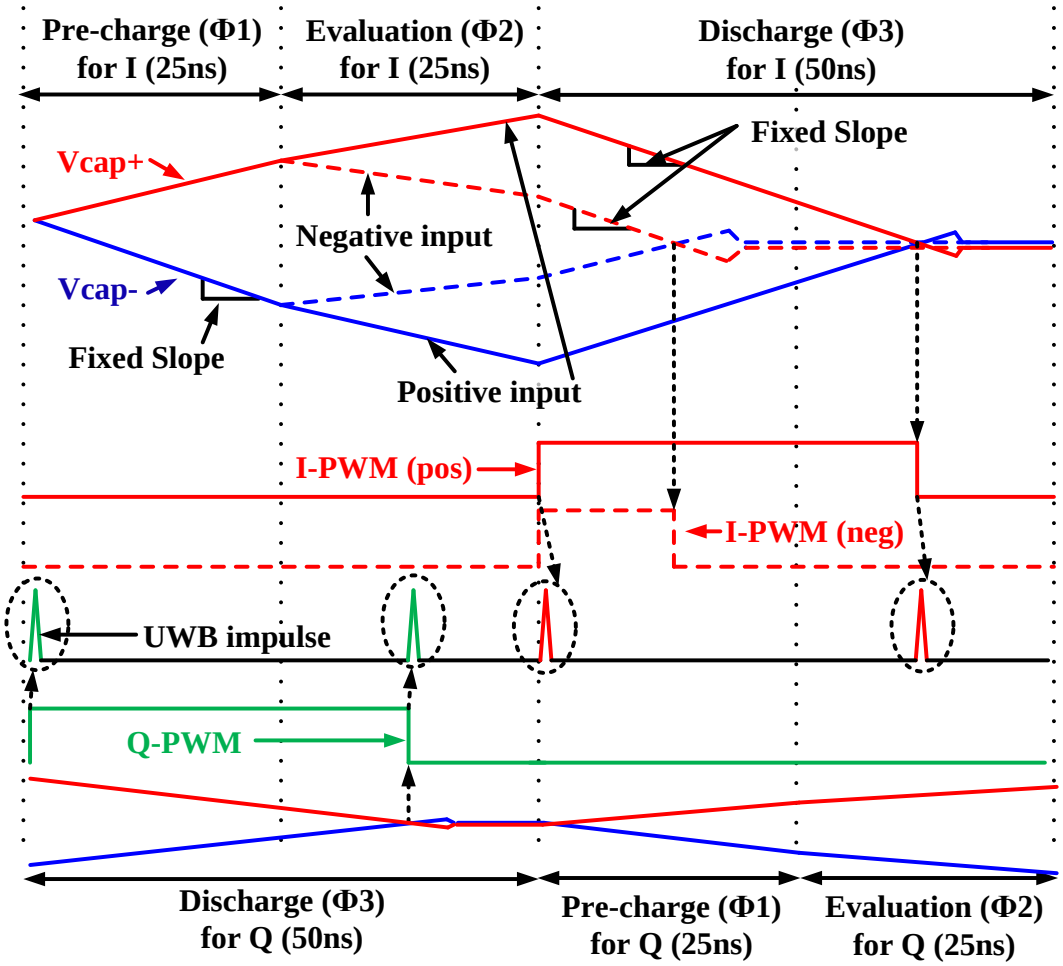
(OTA) converts the differential input voltages which are generated from the STDC to a pair of differential currents, and the following switches mix the current signals and the LO signals from I and Q outputs of the clock multiplier. Biquad TIAs following the mixer switches not only convert the mixed currents to differential voltage signals but also remove the high-frequency image signals. Since the expected STDC output range is ±200 mV and a valid input range for the PWM block is ±400 mV, as explained in chapter 3, the mixer has a conversion gain of 6 dB. To achieve 7-bit resolution, the output noise of the mixer should be less than 0.5 LSB (1.56 mV), which defines the noise specification for the mixer design and performance.

4.2.7 Impulse radio pulse width modulator (IR-PWM)

Fig. 4.6a shows the triple-slope pulse-width modulator and the IR-PWM transmitter. As shown in Fig. 6b, in the 25 ns pre- charge phase (Φ1), inputs of an OTA are connected to reference voltages, resulting in *Cap+* and *Cap-* to be charged with a fixed slope at the



(a)



(b)

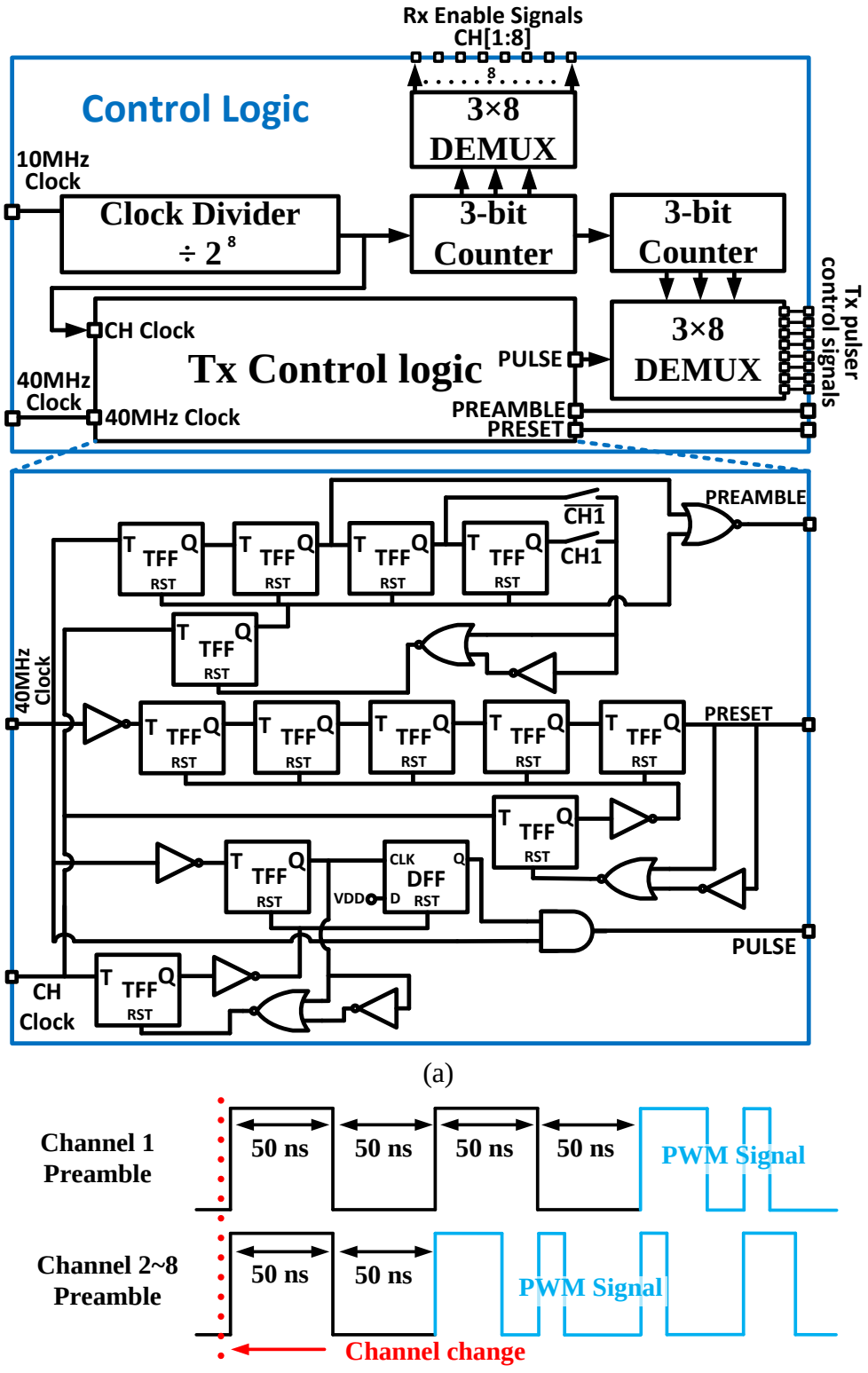
Figure 4.6. (a) Schematic diagram of a triple-slope impulse-radio pulse-width modulator (IR-PWM), and (b) an operational diagram of the PWM-IR-UWB showing the key waveforms in Fig. 4.6a.

output of the OTA. In the 25 ns evaluation phase (Φ2), the OTA charges or discharges the caps at a rate that depends on the input voltage, and finally, in the 50 ns discharge phase (Φ3), the OTA discharges *Cap+* and *Cap-* with the opposite slope of Φ1. The onset of each PWM pulse is synchronized with the beginning of Φ3 and ends at the point where *Vcap+* = *Vcap-*, resulting in a pulse width directly proportional to the input voltage.

The high sampling rate (20 MS/s) requires the OTA to have a considerable current driving capability, requiring us to avoid the resulting voltage dropout across switches in our earlier design [96]. To maintain high resolution at this sampling rate, the PWM should be highly linear, which is achieved by using a source degenerated input differential pair, adopted at the input of the OTA. If the voltage difference at the input of the differential pair is large, one of the input devices is turned off and the OTA tail current (I_{ss}) flows entirely through the other device [98]. Therefore, input voltage difference at the input of the PWM block is limited to ± 400 mV to prevent such a nonlinearity. The I-PWM and Q-PWM signals are combined to double the wireless link bandwidth, before being fed into the IR-UWB block in Fig. 6a, which generates sharp pulses (0.8 ns in width) at the rising and falling edges of the combined PWM signal. An all-digital PA drives the UWB antenna with the IR-UWB impulses, which alternately represent the beginning and the end of the I-PWM and Q-PWM pulses.

4.2.8 Digital controller

The digital control block for the IVUS front-end is illustrated in Fig. 4.7a. The TIAs are multiplexed since we use only one U-Rx channel at a time in this particular implementation of the synthetic-aperture imaging method. Considering that a CMUT transmits a pulse and we receive the echo signal reflected from the target, the active channel



(a)

(b)

Figure 4.7. (a) Schematic of the controller block for the guidewire IVUS imaging system; (b) Waveforms of the preamble signals for the combined PWM output to mark the onset of every channel and for indicating channel-1.

duration should be longer than the round trip duration of the acoustic wave. Since c = 1540 m/s, the travel time for imaging a target at 1 cm would be 13.47 µs. Considering the 10 MHz reference clock of this system, we set the channel duration at 25.6 µs (CH clock), which is easy to generate by dividing the 10 MHz power-carrier signal by 256 using eight D-type flip-flops. The divided clock selects the U-Rx and U-Tx channels from 1 to 8, utilizing a 3-bit counter to control the U-Rx channels followed by another 3-bit counter to control the U-Tx channels. Enable signals for U-Rx and U-Tx are connected to each TIA and pulser that control the activated CMUTs, respectively. The U-Tx control logic generates U-Tx pulses with 12.5 ns width, which are suitable for 40 MHz CMUTs, as well as a preset signal with 400 ns width at the rising edge of the CH clock.

To recognize switching between channels on the IR-Rx side, a preamble is added to the PWM data stream at the onset of every channel. Since PWM pulses are always narrower than 50 ns during normal operation, we have designed the pattern of preamble signal as a combination of two 50 ns pulses with a 50 ns interval. In addition, channel-1 is assigned a unique preamble, as shown in Fig. 4.7b, to be differentiated from the other channels on the IR-Rx side.

4.3 Measurement results

A proof-of-concept guidewire IVUS SoC prototype was fabricated in the TSMC 0.35-µm 5 V standard CMOS process, occupying 4.07 mm2, as shown in Fig. 4.8. Here we present key measurement results.

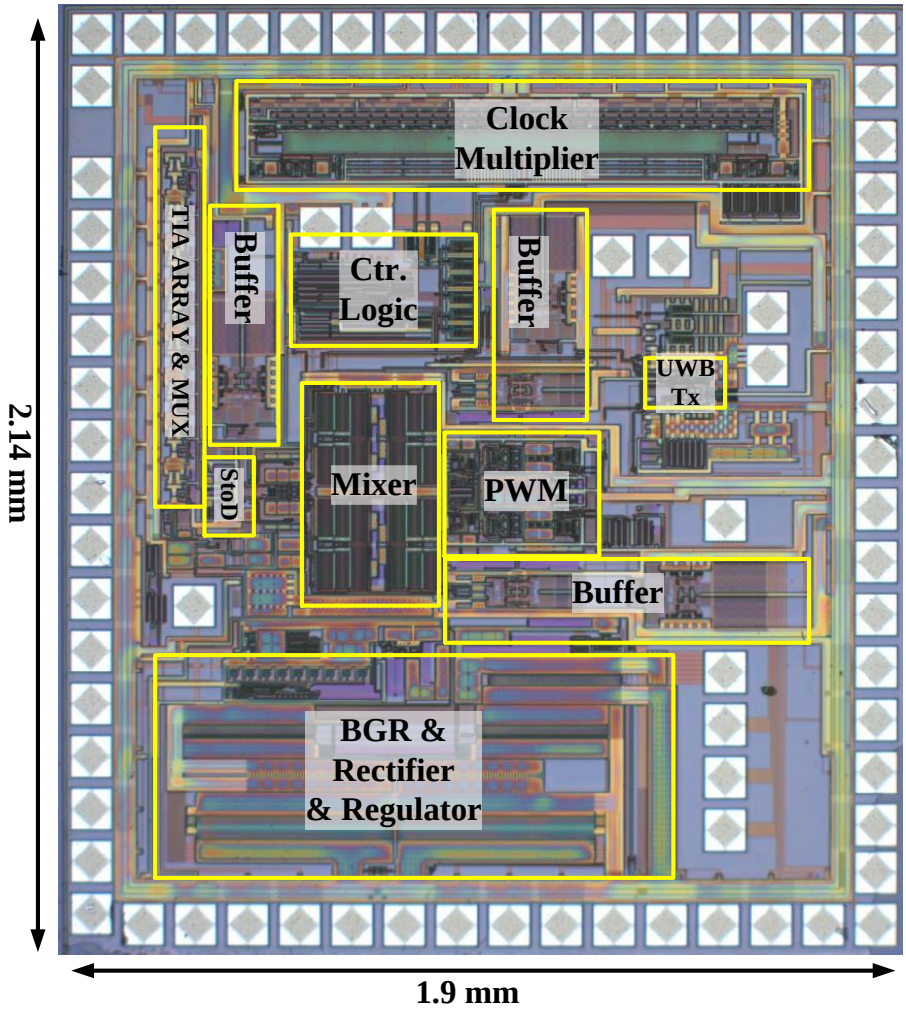


Figure 4.8. Die photomicrograph of the prototype guidewire IVUS-SoC, fabricated in a 0.35-µm standard CMOS process.

4.3.1 Transimpedance Amplifier

To characterize the TIAs, we used a series RC (1 MΩ and 100 pF), shown in Fig. 9, to generate current signals from a voltage source. Since the 1 MΩ resistor is much larger than the TIA input impedance, the TIA input current is proportional to input voltage and inversely proportional to the series resistance. We added on-chip buffers following TIAs to reduce the effects of measurement tool parasitic and improve the accuracy of

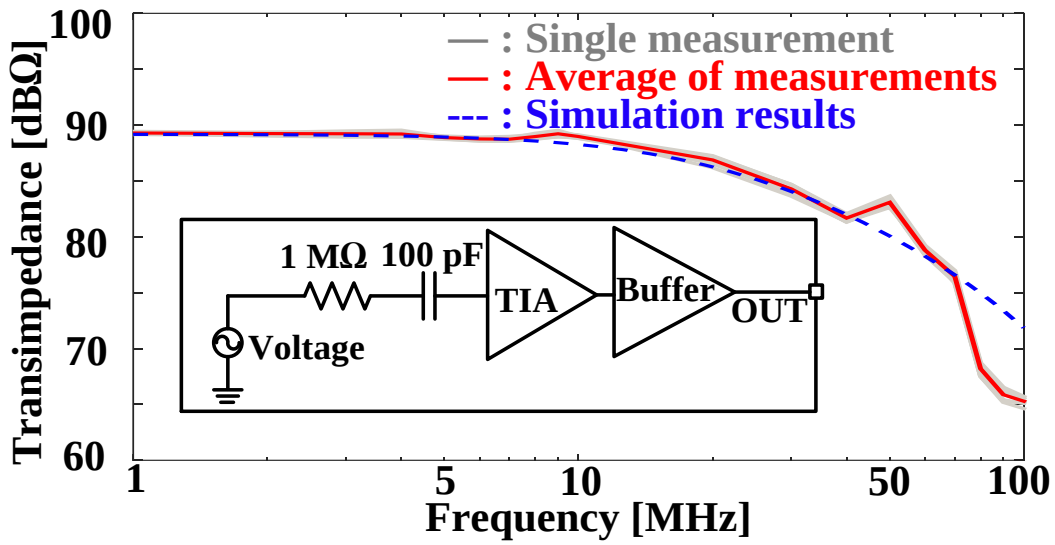
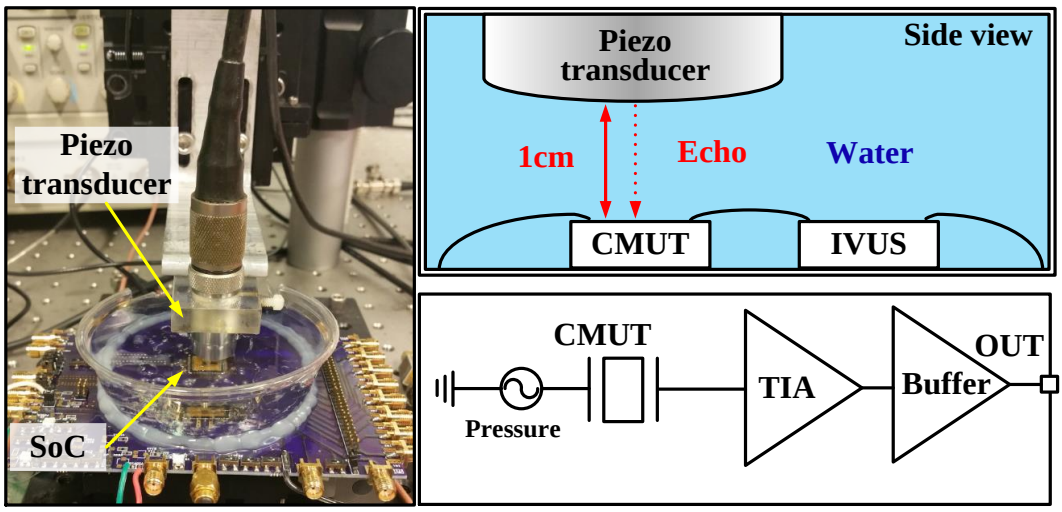


Figure 4.9. (Inset) block diagram of the TIA measurement setup, and measurement results indicating the TIA frequency response.

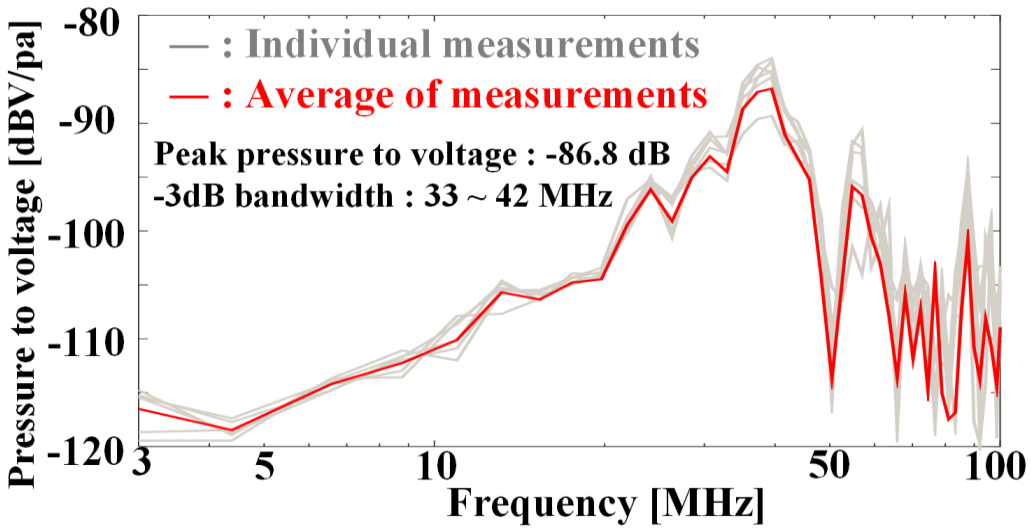
measurements. Fig. 4.9 shows the frequency response of all 8 on-chip TIAs, their average, and post-layout simulation results, which indicate an average transimpedance and bandwidth of 28.5 kΩ and 20 MHz, respectively.

To measure the actual spectrum of the pressure to voltage conversion ratio of the TIA + U-Rx CMUT, an ultrasonic pressure signal was generated using a precision piezoelectric transducer (V358-SU, Olympus) in water, as shown in Fig. 4.10a, and the pressure input at the CMUT position was calibrated using a broadband hydrophone (HGL-0085, Onda, Sunnyvale, CA). Measurements, shown in Fig. 4.10b, indicate that the CMUT + TIA has a -3dB bandwidth of 33-42 MHz with peak pressure to voltage conversion ratio of -86.8 dBV/Pascal. Therefore, even though the TIA by itself had a narrow bandwidth (DC -20 MHz), TIA + CMUT have enough bandwidth to cover the echo signal spectrum (35-40 MHz).

We measured the output noise of the TIA + CMUT in water with a spectrum analyzer (N1996A, Agilent) using the setup described in section 4.4.4. We also measured



(a)



(b)

Figure 4.10. (a) Measurement setup for testing the TIA along with CMUT, (b) CMUT + TIA measurement results.

the noise spectral density at the CMUT center frequency, 40 MHz, without and with a CMUT to be 28 nV/√Hz and 89 nV/√Hz, respectively. Considering the transimpedance of the TIA, which is ~12 kΩ at 40 MHz (see Fig. 4.9), the input referred current noise of the TIA is about 2.3 pA/√Hz, which is 53% larger than simulation results. We anticipate that with better packaging and proper integration of the CMUT + SoC, and improved shielding

around the measurement setup, this difference that is attributed to the external interference to be reduced.

4.3.2 Clock Multiplier

The DLL-based clock multiplier, which generates 40 MHz square waves from the 10 MHz power carrier, was tested through an on-chip buffer. The measured clock jitter peaked at +280 ps/-200 ps with an RMS value of 114 ps. This was larger than the 100 ps peak jitter design target, which is needed to achieve 7-bit resolution in the ATC block. We attribute this to non-uniformity of the inverters in the delay chain of the DLL. The 40 MHz square wave duty cycle varied from 49.2% ~ 50.8%.

4.3.3 Analog-to-Time Conversion and Pulse Width Modulator

In order to avoid additional parasitic capacitance at the mixer output, which loads the mixer and results in additional noise in the ATC (PWM generator) block, we implemented an identical ATC block on the prototype ASIC with the exact same layout for

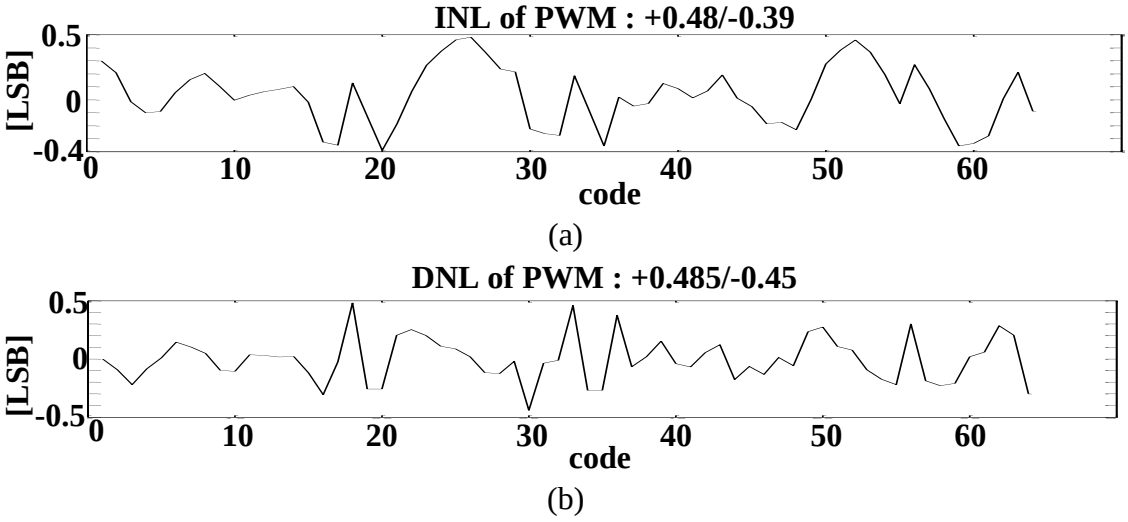
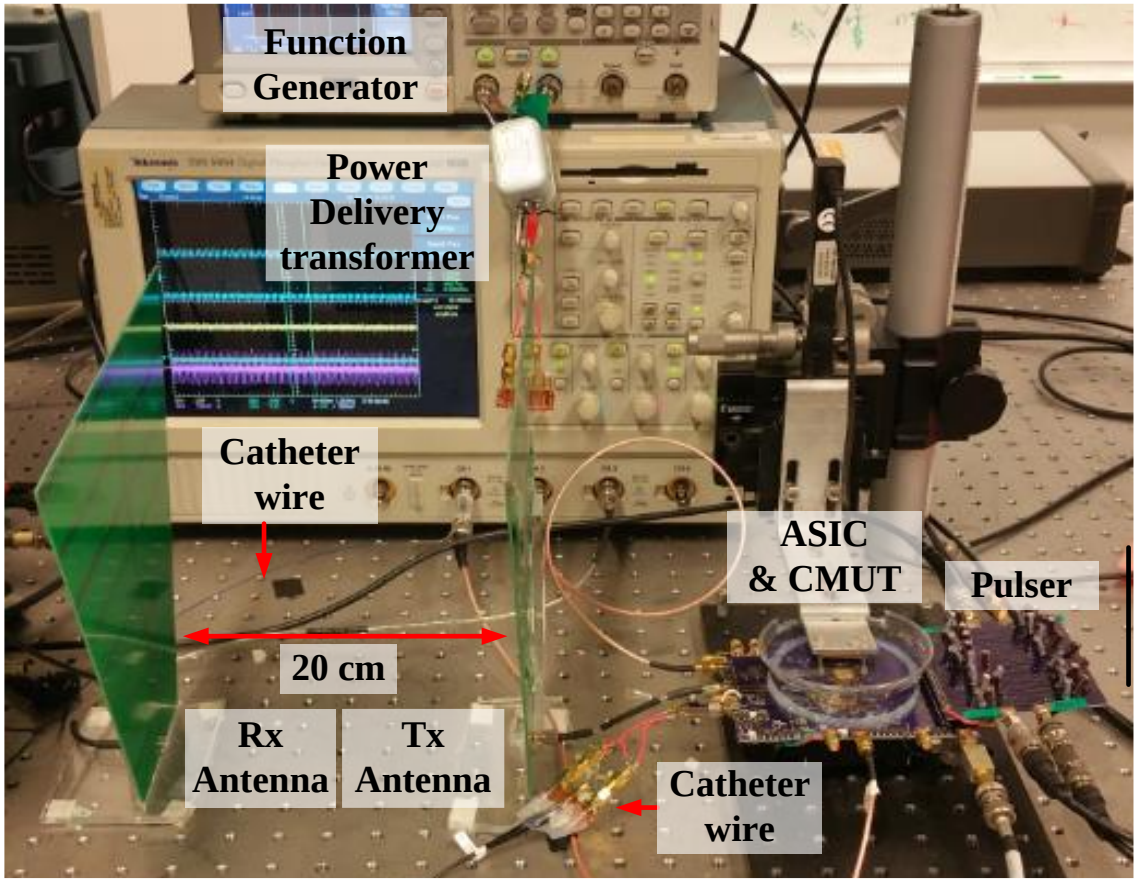


Figure 4.11. Measured (a) INL and (b) DNL of the analog-to-time converter (ATC) output.

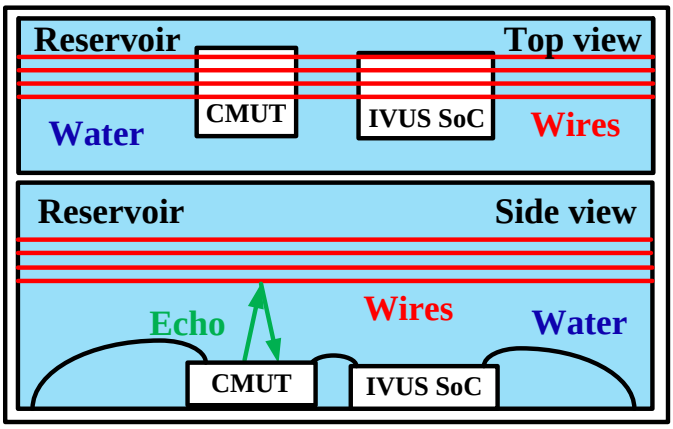
characterization only. We measured the integral non- linearity (INL) and differential nonlinearity (DNL) errors of the ATC block by applying a ramp input to the separate ATC block and capturing the resulting PWM pulse width, using a 1.5 GHz wideband oscilloscope at 20 GS/s. The PWM pulse width was then calculated in MATLAB and led to measurement results in Fig. 11, which show peak INL of +0.48 / -0.39 LSB and peak DNL of +0.485 / -0.45 LSB with 6-bit resolution at 20 MS/s (less than 0.5 LSB). Therefore, the equivalent data rate out of the ATC block is ~120 Mb/s. The effect of noise on reference voltages and limitations in the linearity of the OTA in the ATC block (see Fig. 4.6), and the jitter of the clock multiplier seem to be the main reasons for limiting the ATC resolution to 6 bits.

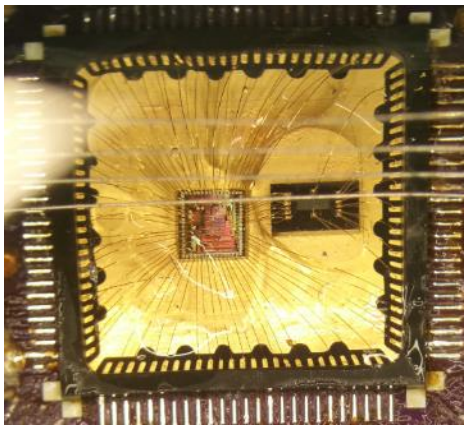
4.3.4 System Level Measurements

Fig. 4.12 shows the experimental setup used to verify the overall system functionality. It includes a function generator (AFG3102, Tektronix), which generates the 10 MHz power carrier and delivers it through a wideband transformer for isolation, followed by a pair of AWG 42.5 wires (58 μm in diameter) taken from a 7-wire 2.4 m long commercial IVUS catheter (Eagle Eye Platinum Catheter, Volcano, San Diego, CA). A 100-pin QFN package houses both the interface SoC and 12-element CMUT imaging array, where the wirebonds near the perimeter of the package are covered with epoxy to prevent them from bending and creating short-circuits. The entire package is then made water resistant by a 3 μm layer of Parylene-C coating by placing the PCB in the Parylene coating chamber for 60 min at room temperature. A cylindrical plastic ring, 8 cm in diameter, was also glued on the PCB around the QFN package to create a small water or oil basin.



(a)





(b) (c)

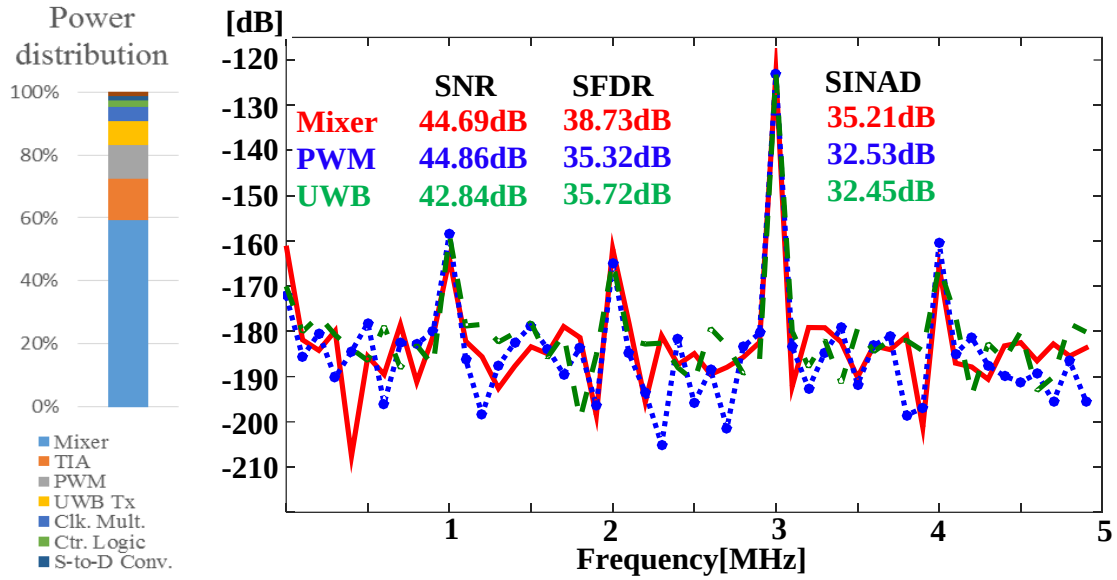
Figure 4.12. (a) System level measurement setup for the prototype guidewire IVUS SoC; (b) Simplified diagram of setup from top and side views; (c) Top view of the SoC and CMUT assembly, wire-bonded together in QFN package.

Because of the relatively large feature size of the 0.35-µm CMOS process, the SoC ability in generating narrow and sharp IR-UWB impulses in this proof-of-concept

prototype was limited to lower frequency content in the 200-800 MHz range. Hence we used a large pair of log-periodic antennas (WA5VJB, Kent Electronics, Sugar Land, TX) with 20 cm separation between the SoC IR-Tx output and the external IR-Rx to cover this band. As mentioned earlier, to monitor the waveforms from each major block output while minimizing the effect of measurement tool on the system performance, we included several on-chip buffers, powered by a separate supply rail.

An 18 Ω current-sense resistor was added after the isolation transformer to measure its instantaneous output power by multiplying the current in this resistor and voltage difference across the transformer output. This value was then used to calculate the RMS power, which was measured 107.4 mW. The power and voltage at the output of the rectifier were 61.05 mW and 3.7 V, respectively. Out of these, the regulator supplied the rest of ASIC with 52.8 mW at 3.3 V, resulting in an overall power transfer efficiency of 49.1% across the IVUS catheter and PMIC block of the interface SoC. The power distribution of the system is shown in Fig. 4.13a. To achieve required noise level, the mixer consumes about half of the system power consumption.

Primary system performance measurement was conducted with a single-tone test at 37 MHz, which is the center frequency of the CMUT under test. In MATLAB simulations, the peak current level from the CMUT was estimated at 3 µA, when the pulse echo signal reflects from the water-air interface at 5 mm depth, which shows a reflection coefficient of -0.005 dB. Hence, we generated a 37 MHz 3 µA current signal using the voltage source and series RC (1 MΩ and 100 pF) combination shown in Fig. 4.9a. The SNR and SFDR were measured at the mixer output through its on-chip buffer. The PWM signal was probed on the IR-Tx side through a coaxial cable, while the PWM-IR-UWB signal was wirelessly



(a) (b)

Figure. 4.13. (a) Power distribution of the system, and (b) single-tone measurement results of the mixer, ATC, and wireless PWM-IR-UWB output signals.

transmitted through the log-periodic antenna pair. The SNR (exclude harmonic distortion) of the signal at the mixer, PWM, and UWB outputs were 44.69 dB, 44.86 dB, and 42.84 dB SNR, respectively, without averaging, while the SFDR of the same signals were 38.73 dB, 35.32 dB, and 35.72 dB, respectively. The measured signal to noise and distortion (SINAD) ratio of the overall system was 32.45 dB that indicates 5.1-bit ENoB. Since PWM samples are taken by charging a pair of capacitors within 25 ns, the ATC block operates like a low-pass filter with 9 MHz bandwidths [72]. Therefore, the ATC reduces high-frequency noise, and shows a higher SNR compared to the mixer output, as shown in Fig. 4.13b. These results are significant as they show that when the interface is changed to a blood-tissue interface with -40 dB reflection coefficient [99], the system can still provide adequate SNR for imaging.

We designed an off-chip eight-channel pulser, shown in Fig. 4.12 using HV MOSFET drivers (MD 1213, Microchip), HV MOSFETs (TC6320, Supertex Inc.), and

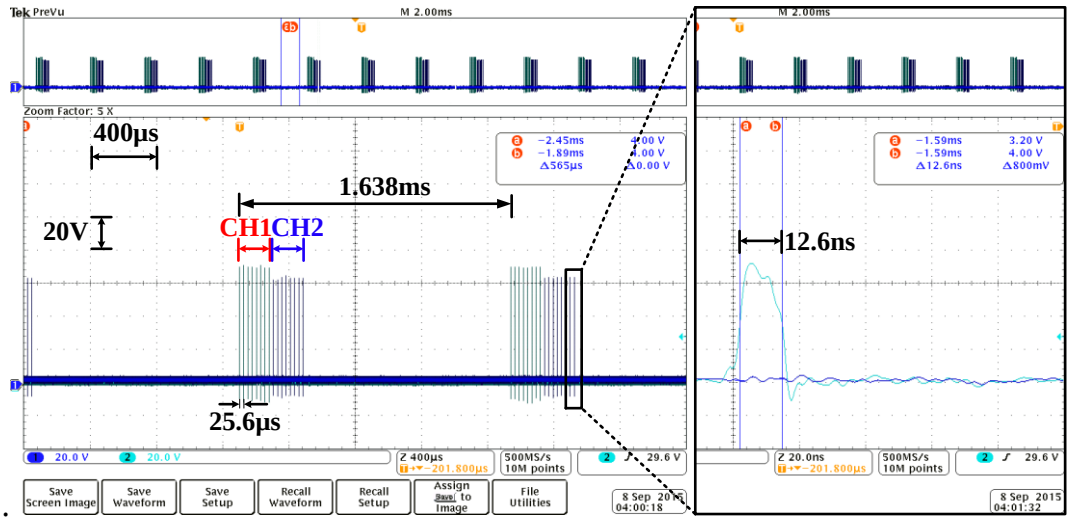
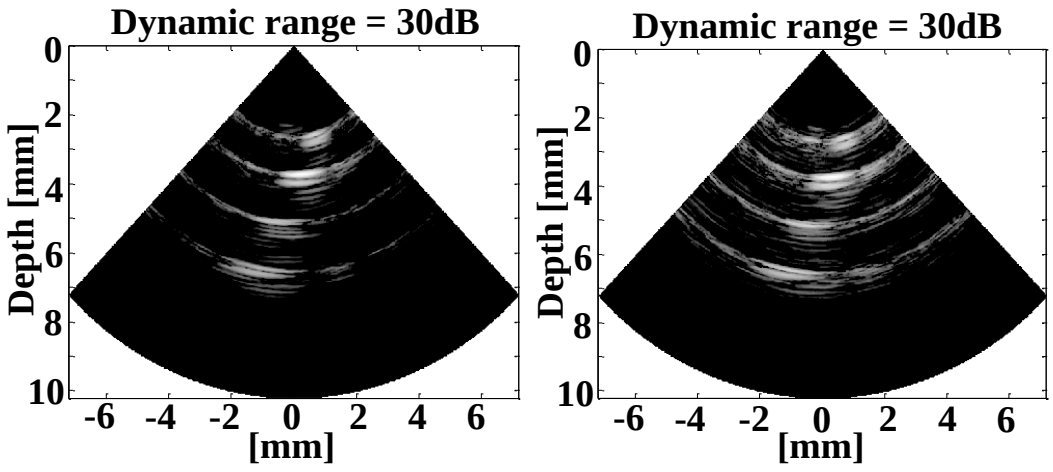


Figure 4.14. Measurement waveforms on the U-Tx side showing the burst of 8 pulses generated by the on-chip digital control block and amplified by the off-chip pulser to drive CMUT for two adjacent channels.

protection diodes (BAV99, NXP Semiconductor) to complement the U-Tx control logic on the interface SoC. The control logic generates a 12.5 ns pulse with 3.3 V amplitude, as mentioned in section III.H, and the pulser boosts it to 60 V. One channel fires every 25.6 µs and after eight firings, the active U-Tx is switched to the next channel, as shown in Fig. 4.14.

4.3.5 Imaging a Four-Wire Phantom

Imaging experiments were performed using a setup as shown in Fig. 4.10. We used four 38-AWG metal wires (101 µm in diameter), immersed in water and diagonally located above the CMUT array at different depths as the imaging phantom. Six elements of the array were used as U-Tx and the other 6 were used as U-Rx in a staggered 1-D array geometry, suitable for performing synthetic phased array processing to form the images. We reconstructed the images offline using both the PWM output signal through a coaxial cable (Fig. 4.15a), and the PWM-IR-UWB signal through the wireless link (Fig. 4.15b),



(a) (b)

Figure 4.15. Reconstructed images from the received signal of the four wire target imaging experiment: (1) PWM output directly probed through a coaxial cable and (b) PWM-IR-UWB signal received through the wireless link.

showing the full functionality of the prototype guidewire IVUS SoC. The PWM-IR-UWB signal was transmitted across the identical log periodic antennas that were placed 20 cm apart. The received signal was recorded by a wideband oscilloscope and reconstructed in MATLAB, which also down converted the IR-UWB signal, detected the rising and falling edges of each pulse, and measured the width of each pulse with 50 ps resolution in the received PWM signal.

All images have 30 dB dynamic range and clearly show all four wires located up to a depth of 7 mm abovethe IVUS array. The dynamic range is lower than desired because of the non-ideal operation of the CMUT array and the mechanical and electrical noise in the experimental setup, limiting the SNR of the individual pulse-echo signals to only 15 dB. Beamforming, on the other hand, improved the dynamic range by ~15 dB [90]. In the images in Fig. 4.15, the axial spreading is more than expected due to extended ultrasonic echo signals following the main echo because of acoustic crosstalk and lateral resolution is limited by the staggered array structure. These drawbacks can be significantly reduced

and the performance can be improved by applying a coating material to suppress surface acoustic waves in CMUT array design [100]. Specification of the first guidewire IVUS prototype SoC has been summarized in Table 4.1, and compared with some of the recent ultrasound interfacing ASICs in the literature.

Table 4.1 - Guidewire IVUS interface electronics benchmarking

	[94]	[23]	This work
CMOS Technology	0.35 µm	0.35 µm	0.35 µm
Power consumption (mW)	26	0.8*	52.8
Power-carrier frequency	-	-	10 MHz
Power-transfer efficiency	-	-	49.15%
Rectifier output voltage	-	-	3.7 V
Supply Voltage	3.3 V	3.3 V/ 25V	3.3 V
TIA Bandwidth	45 MHz	40 MHz	20 MHz
TIA Transimpedance	100 kΩ	200 kΩ	28.5 kΩ
Noise of TIA (nV/√Hz)	150 (@40 MHz)**	62 (@20 MHz)	28 (@40 MHz)
TIA + CMUT Bandwidth	-	-	33 ~ 42 MHz
TIA + CMUT Noise (nV/√Hz)	-	-	89 (@40 MHz)
Conversion gain of mixer	10.1 dB	-	6 dB
Mixer Bandwidth	2 MHz	-	7 MHz
RMS of clock jitter	443 ps	-	114 ps
PWM sampling rate (MS/s)	2 ×10	-	2 ×10
ATC Resolution	5 bits	-	6 bits
System ENoB			5.1 bits
IR-UWB Spectrum	-	-	0.2 - 0.8 GHz
System effective data rate	100 Mb/s	-	100 Mb/s

*Power consumption of one TIA.

**This work only provided simulation results on noise measurement.

CHAPTER 5. REDUCED-WIRE TRANSCEIVER FOR GUIDEWIRE IVUS SYSTEM

As we mentioned previously, the Rx CMUT requires high DC bias, and the Tx requires high voltage pulse. However, with the TSMC 0.35-μm standard CMOS process, which we demonstrated Rx-only wireless read-out system for guidewire IVUS system, we could not implement Tx part of the system. Therefore, we designed the guidewire IVUS system with TowerJazz 0.18-μm power management process, which provides high voltage lateral double-diffused MOSFET (LDMOS), operating up to 60 V.

5.1 Integrated transceiver for high-frequency CMUT-based IVUS system

5.1.1 Integrated transceiver for high-frequency CMUT-based IVUS system

The overall system block diagram is shown in Fig. 5.1. In this system, every element in a CMUT array is connected to a single transceiver, which consists of a TIA and a pulser. Since we adopted a synthetic aperture beamforming for the system to reduce the power consumption and interconnection, only one or two CMUT elements are activated for Tx and Rx. The system started to gather the echo signal from the left-end CMUT element both as Tx and Rx and sequentially changes the Rx CMUT element to the right one. After gathering the echo signal from the right-end element as Rx, repeat the same process with the Tx CMUT element next to the previously activated Tx CMUT element until gathering signals from the right-end Tx CMUT elements. Accordingly, after 256-times of transmitting and receiving (from 16 channel 1-D TRx CMUT array), by mapping the echo signals on 2-D space, we construct an image. Because our target distance is from

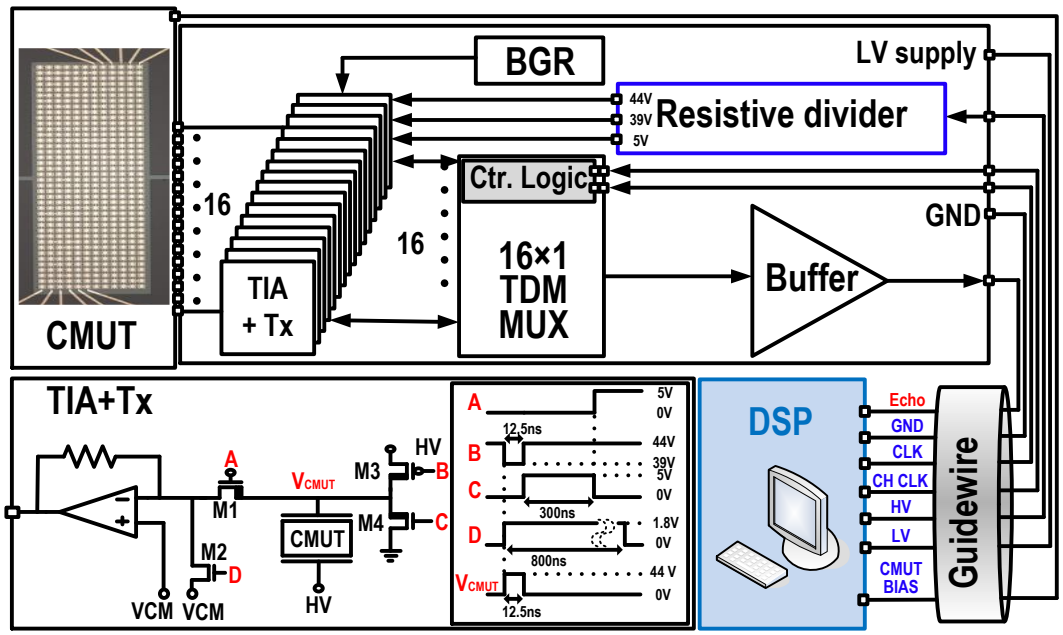


Figure 5.1. System block diagram of the integrated transceiver for high-frequency CMUT-based IVUS system.

0.7 mm to 1 cm, one transmitting-receiving activity takes 25.6 μs and more than 6.5 ms for an image of the 1-D array. Thanks to synthetic aperture imaging, we receive the pulse echo signal from only one Rx CMUT element among 16 elements, a buffer transfers the TIA output of the Rx elements to the external side by time-division multiplexing (TDM). A digital control logic generates not only the control signals for TDM but also control signals for a pulser (A, B, C, and D in Fig. 5.1) by using an external clock. The external clock is a 32-burst 40-MHz square wave (*CLK*), which is synchronized with the rising edge of channel clock (*CH CLK*), 39.07 kHz square wave.

When the pulser generates a pulse, high voltage switch M1 is open (A=0 V), M3 pulls up (B=39 V) the top electrode of the CMUT membrane (V_{CMUT}) to high voltage (HV) of 44 V for 12.5 ns (pulse width). M4 pulls down (C=5 V) V_{CMUT} to ground for 300 ns. At the same time, M2 applies the common mode voltage *(VCM*) at the TIA input to prevent a high-peak feedthrough voltage from V_{CMUT} (D=1.8 V). After the transmitting is finished,

M1 is closed (A=5 V), and M3 and M4 are turned off to prevent current leakage through M3 and M4 while Rx CMUT receives an echo signal. Accordingly, we force the current output from the Rx CMUT to flow to the TIA input.

Since HV supply is far higher than LV supply, it requires an on-chip DC-DC converter to share an interconnection for both supplies. Considering the size limitation of the system, DC-DC converter, which requires large size inductor or capacitor [101]-[103], is too large to implement on the chip. Therefore, we separately provide HV and LV supplies to the chip. Since the pulser requires three different voltages (5 V, 38 V, and 44 V), a resistive voltage divider is used. Although, in this prototype, the resistor divider was implemented on the PCB, not the chip, to adjust the voltage for testing, it can be easily implemented on the chip with a small area. Eventually, the CMUT bias and HV supply will be the same, but, so far, CMUT requires higher DC bias for an operation which requires another interconnection for it.

5.1.2 Measurement results

The integrated transceiver for high-frequency CMUT-based IVUS SoC was fabricated in TowerJazz 0.18-μm HV CMOS process occupying an active area of 0.84 mm^2 (Fig. 5.2), and the chip was tested on the setup shown in Fig. 5.3. The SoC consumes 63-

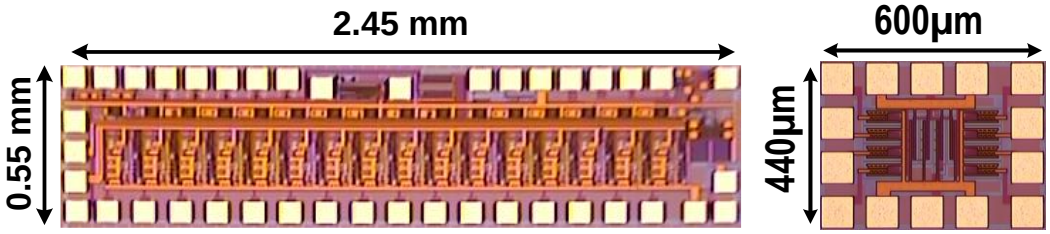


Figure 5.2. Microphotograph of (left) integrated transceiver for high-frequency CMUT-based IVUS system (ASIC) and (right) control ASIC (CTR ASIC).

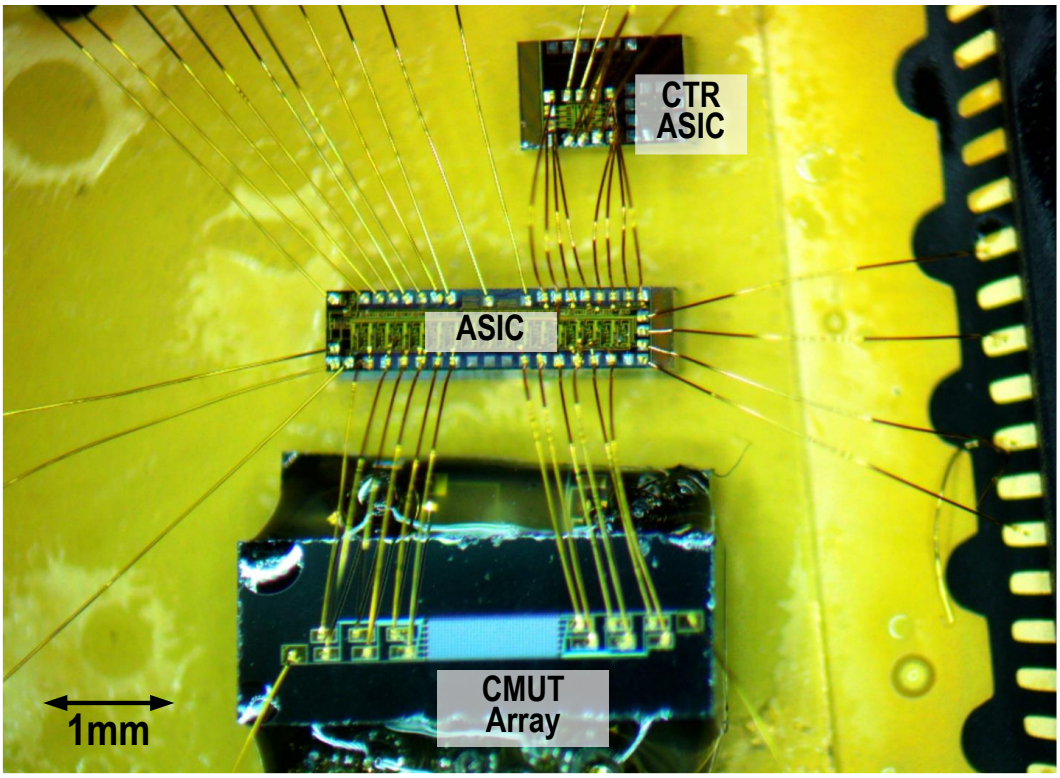


Figure 5.3. Experimental setup.

mW and 88 mW for LV and HV supply respectively. In this experiment, since our target CMUT is not fabricated yet, we used our previous CMUT in [104]. The IVUS system will be eventually merged with four sides looking 1-D phased array, and the TDM control logic should be shared by them. Accordingly, we separated TDM control logic in a small separate chip (Fig. 5.2).

In Fig. 5.4, we showed characterization measurement setup and results of the SoC with the CMUT array with DC bias of 80% of the collapse voltage (80 V) applied on the bottom electrode of the CMUT array. For the receiver characterization (lower Fig. 5.4), we used piezo electric transducer (V358-SU, Olympus) as a Tx and received with a CMUT element (detail specifications are in [104]) followed by TIA and buffer. We measured it in water and subtracted the spectrum of the piezo transducer, which is calibrated with a

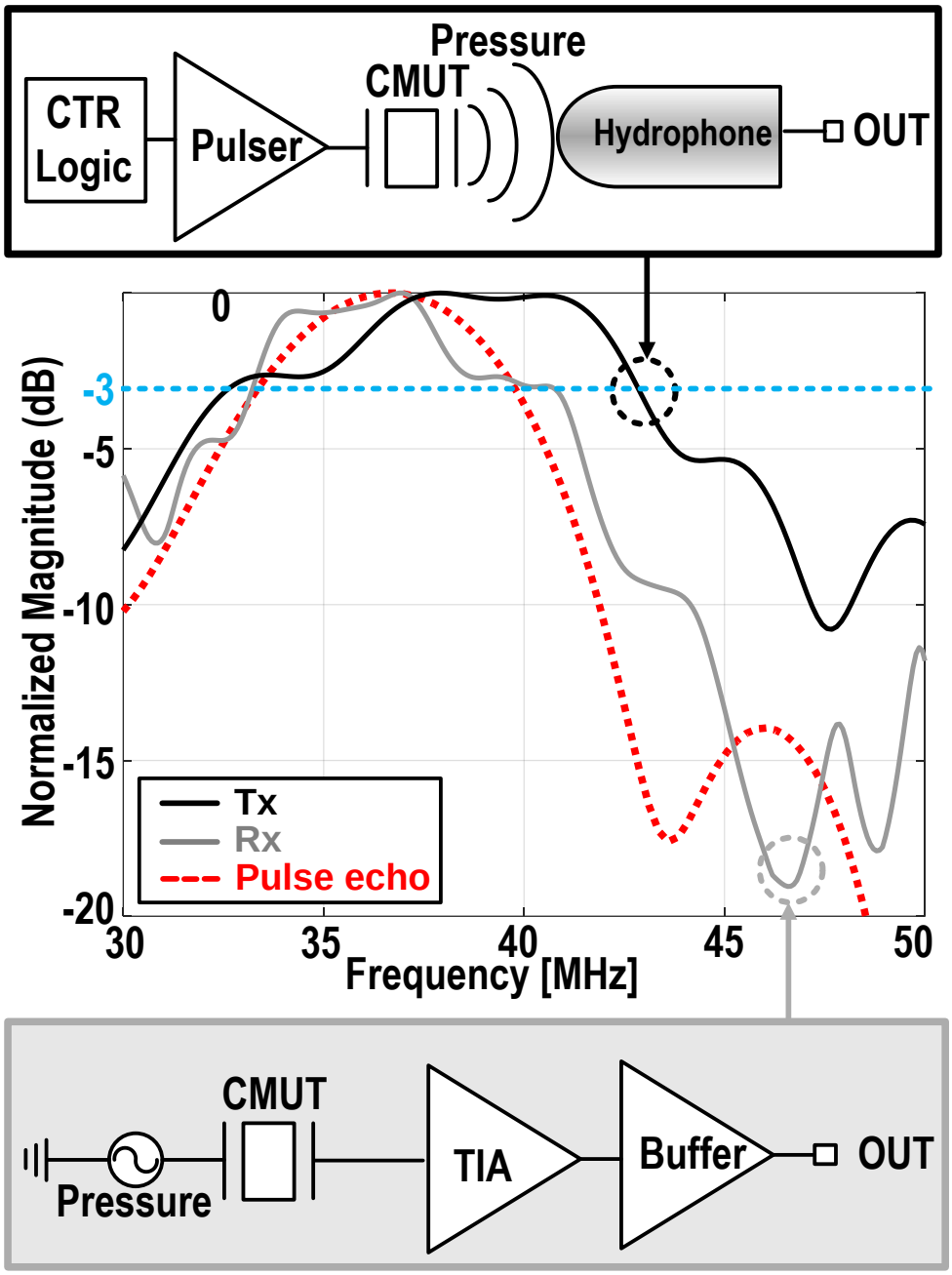


Figure 5.4. Measurement diagram and results of CMUT+SoC characterization.

broadband hydrophone (HGL-0085, Onda, Sunnyvale, CA), from the measured Rx spectrum. The measured spectrum shows -3dB bandwidth of 33 – 40 MHz. For the transmitter characterization (upper Fig. 5.4), we placed Tx CMUT and the Rx hydrophone, the same hydrophone used in Rx characterization, at 1 cm apart from each other, and

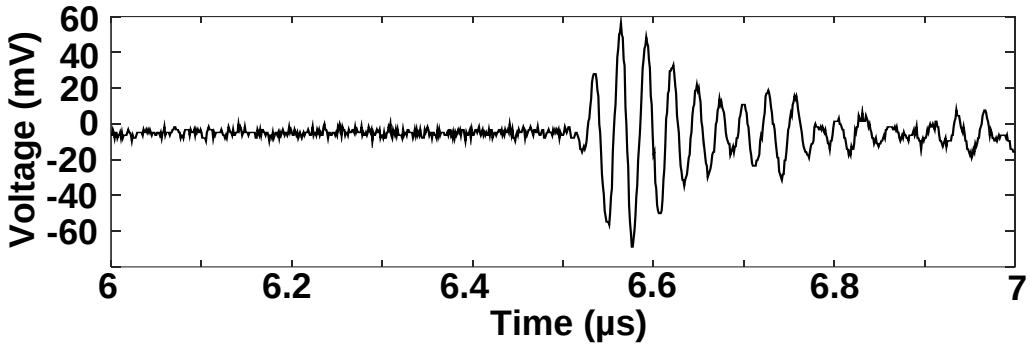


Figure 5.5. Measured pulse echo from a water-air interface with 5 mm distance.

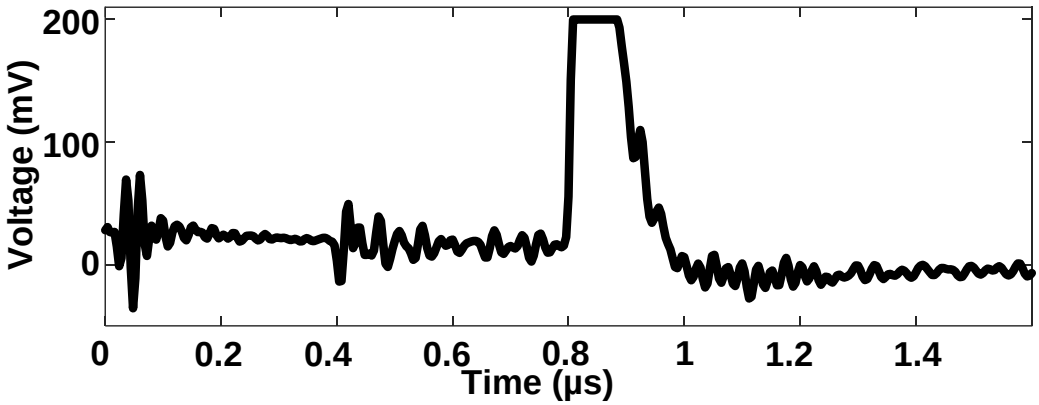
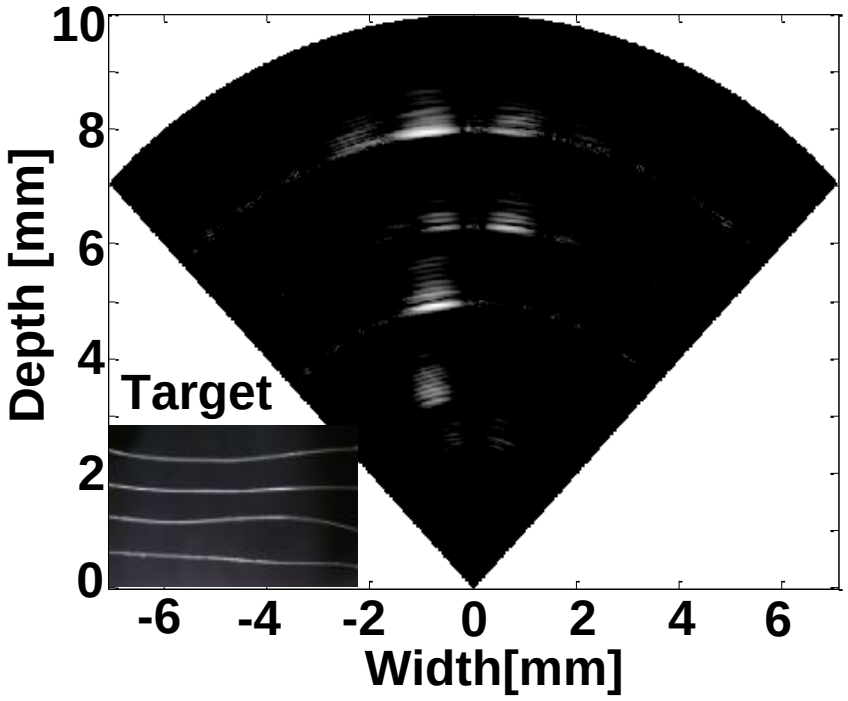


Figure 5.6. Measured waveform at the beginning of receiving operation.

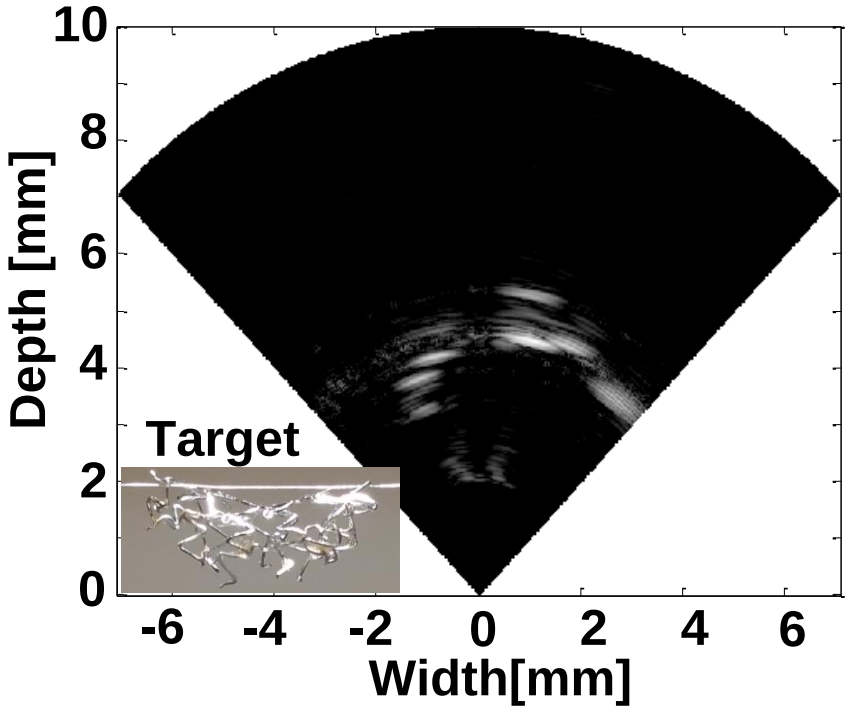
measured the acoustic pressure from the Tx CMUT. The Tx pressure shows -3 dB bandwidth of 32-43 MHz. Fig. 5.5 depicted the transient signal of a pulse-echo measurement with water-air interface with 5 mm distance. The spectrum of the signal shows -3 dB bandwidth of 33-40 MHz (in Fig. 5.4) with SNR of 36 dB. The SNR was calculated by

$$SNR = \frac{Peak\ of\ echo\ signal}{RMS(noise)}. \tag{5.1}$$

Eventually, imaging experiments were performed using a setup shown in Fig. 5.3. We used four 38-AWG metal wires, diameter of 101 μm, immersed in water and vertically located above the CMUT array at different depths as the imaging phantom. Twelve elements of the array were used as T-Rx, by performing synthetic phased array processing



(a)



(b)

Figure 5.7. Reconstructed images from the received signal of (a) the four wire target and (b) stent target imaging experiment.

to form the images. As shown in Fig. 5.6, the receiver was designed to start recording after

750 ns of Tx firing, but it requires additional 120 ns for stabilizing the TIA after the switching. Therefore, the system starts imaging from depth of 760 µm.

The imaging results, shown in Fig. 5.7a, have 30 dB dynamic range and clearly show all four wires located up to a depth of 8 mm above the IVUS array. In addition, we conducted another experiment with a stent. To emulate the situation inside of the artery, we cut the stent in half and opened it to make arc-shape. The results are shown in Fig. 5.7b.

5.2 Reduced-wire guidewire ultrasound imaging SoC

5.2.1 Reduced-wire guidewire ultrasound imaging SoC

To integrate the system on a guidewire, we need to reduce the size of interconnections. The guidewire ultrasound imaging system-on-a-chip (GUISoC) concept shown in Fig. 5.8 achieves this goal by reducing the number of electrical connections and cable requirements obviating the need for a separate catheter. This single-chip real-time imaging system, which fully integrates transmitter/receiver AFE functionalities and performs on-chip signal processing to reduce the cable bandwidth requirements, fits on 0.7mm × 2.5mm footprint, suitable for a 0.035” guidewire.

Fig. 5.8 shows the GUISoC block diagram. To achieve high image resolution, design target for the center frequency of small CMUT was 40 MHz with 10 MHz bandwidth. We designed the electronics for use with a linear array of 16 elements, sized 1mm × 300µm, where each element is used both as transmitter (Tx) and receiver (Rx). Since our CMUT fabrication process is compatible with CMOS process, the array can eventually be post-processed directly on the SoC eliminating the need for padframe and reducing interconnect parasitic [46]. For image formation the chip uses a synthetic

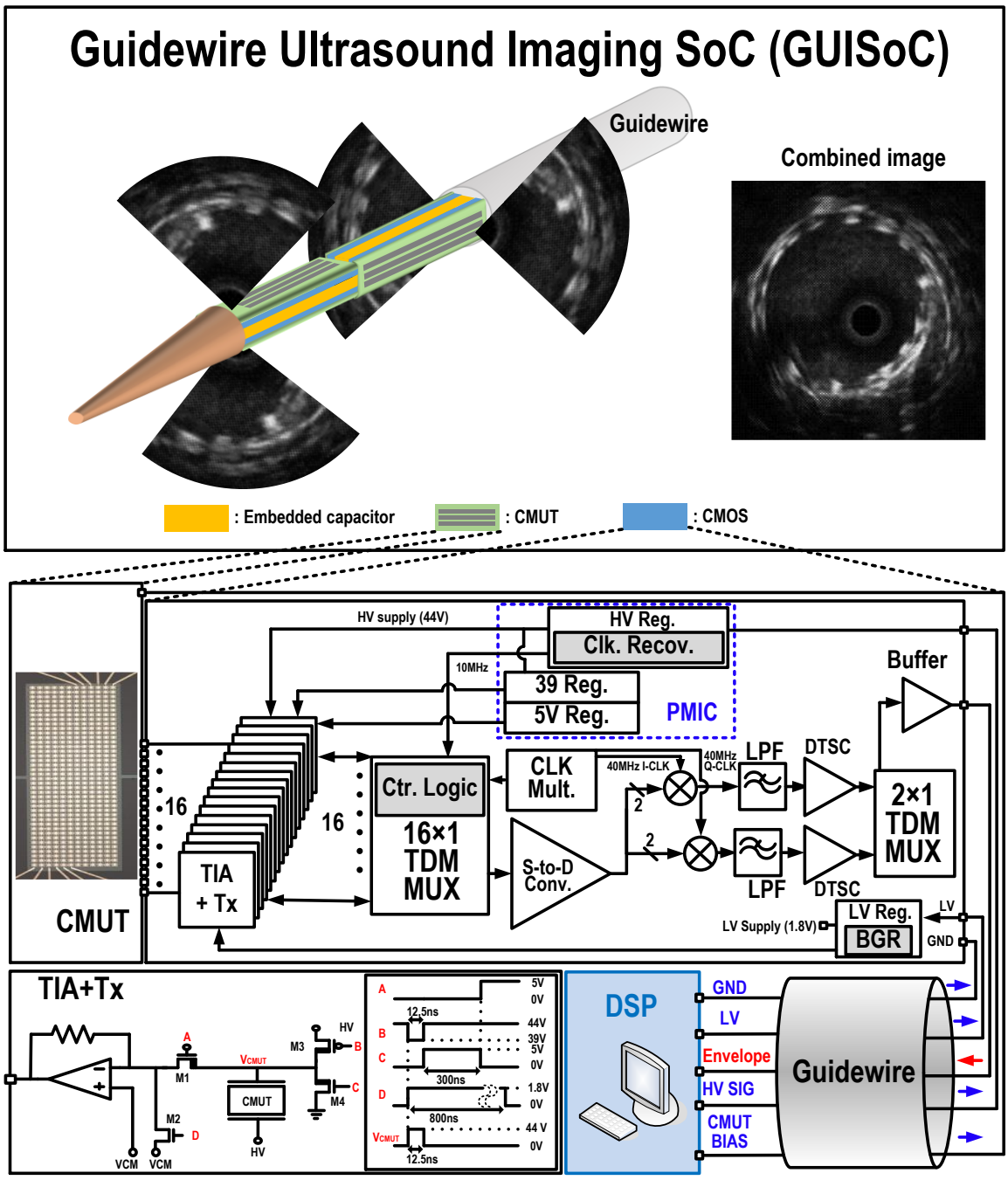


Figure 5.8. Conceptual picture (top) and overall system block diagram (bottom) of the proposed guidewire ultrasound imaging SoC.

aperture imaging scheme which activates only a pair of Tx-Rx elements at a time and sequentially scans all various combinations with time division multiplexing (TDM). Therefore, the GUISoC includes a complete real-time imaging AFE with >30 fr/s frame

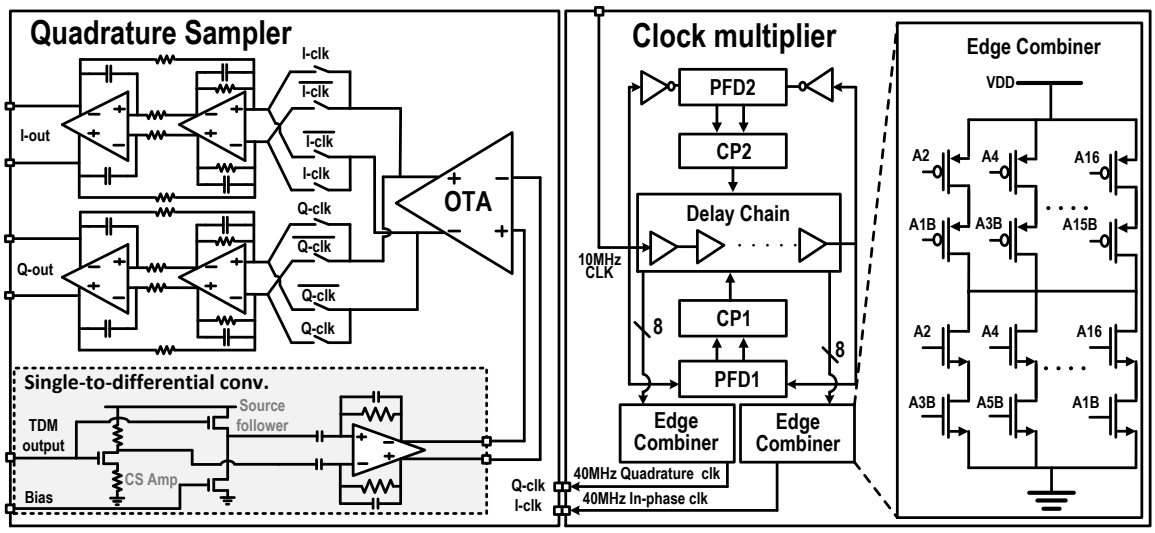


Figure 5.9. Schematic of quadrature sampler (left) and clock multiplier (right).

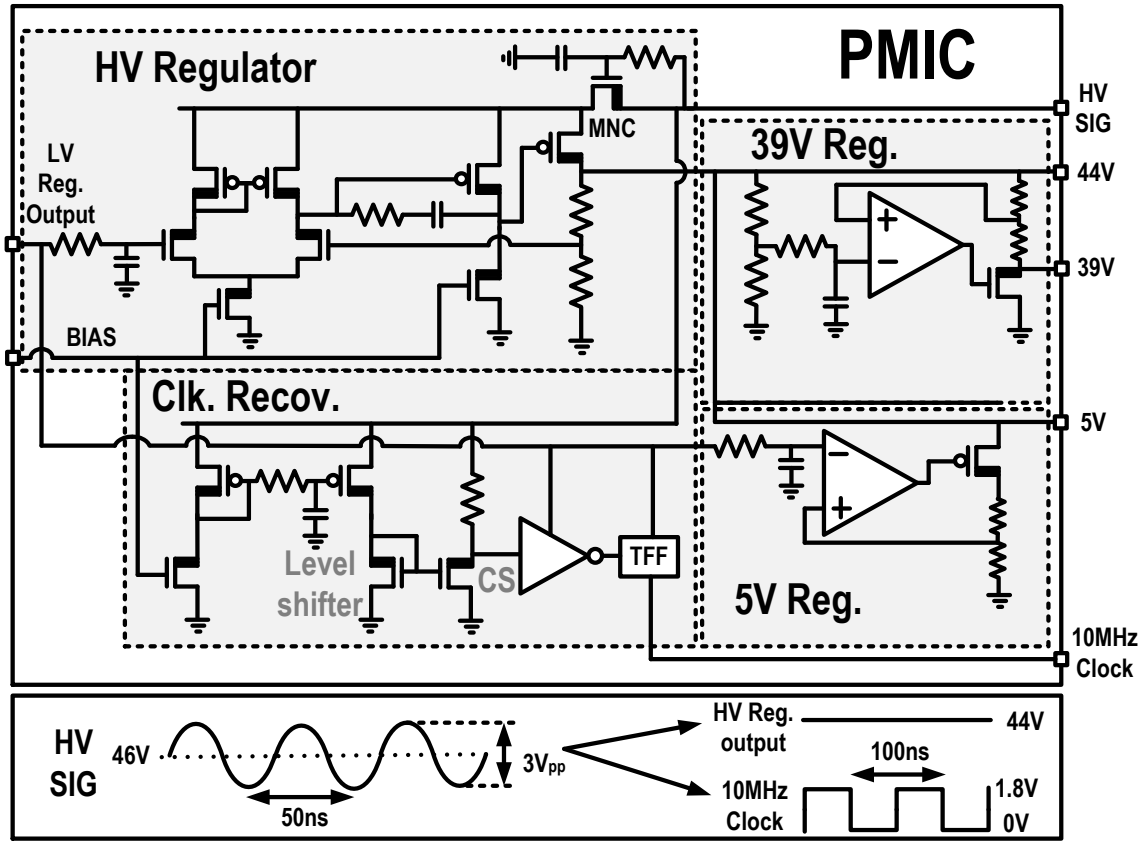


Figure 5.10. Block diagram of PMIC.

rate with as current ultrasound systems and reduces power consumption by disabling all TIAs except for the active CMUT.

A T/Rx switch (M1) isolates transimpedance amplifiers (TIA), which convert the CMUT output currents due to echo signal within 32.7 MHz ~ 37.5 MHz bandwidth to voltage, from a pulser, which generates 44V pulses with 12.5ns pulse width. The SoC uses quadrature sampling for envelope detection as is widely used in US imaging [105]. A dual delay-locked loop (DLL), shown in Fig. 5.9, generates 40MHz in-phase and quadrature phase local oscillator (LO) signals from a 10 MHz clock, which is extracted from the high voltage (HV SIG) power line, and fed into the I-Q direct down-conversion mixers.

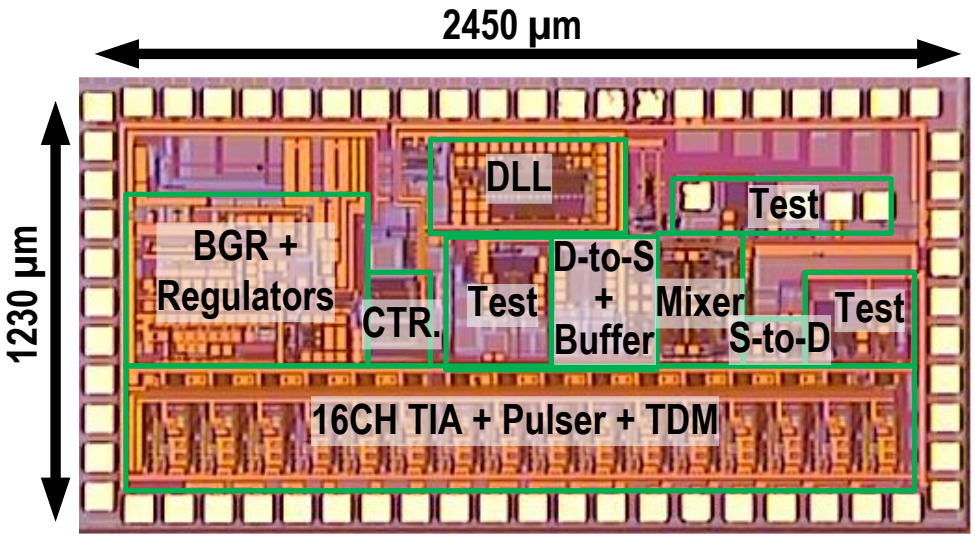
Since the system requires two supplies with a large gap for Tx/Rx (44V/1.8V), considering limited space at the tip of the guidewire, two separate wires (HV SIG/LV) deliver them instead of a step-down converter. To reduce the number of wires, however, a 20 MHz sine wave with $3V_{pp}$ is added to 46 V DC to generate HV SIG, as the input of the HV regulator in Fig. 5.10, which creates a 10 MHz clock and Tx supply (44V) on the chip. MNC in Fig. 5.10 with RC low pass filter isolates the regulator from the AC signal on HV SIG [95]. The A common gate amplifier is used for level shifting followed by a common source (CS) amplifier, inverter, and T-flipflop to generate the 10MHz square wave.

We used resistive feedback transimpedance amplifier (TIA) in the AFE because it is more area efficient compared to capacitive feedback TIA (Fig. 5.8) [96]. The TIA was designed to have 100 kΩ transimpedance with -3dB bandwidth of 20MHz, resulting in 29 - 45 MHz measured bandwidth with the CMUT equivalent model. The target TIA noise level is 41 nV/√Hz at 40MHz, below the CMUT noise level. Although TIA is separated from pulser by M1, the coupling of large pulses from a firing CMUT in Tx mode onto other

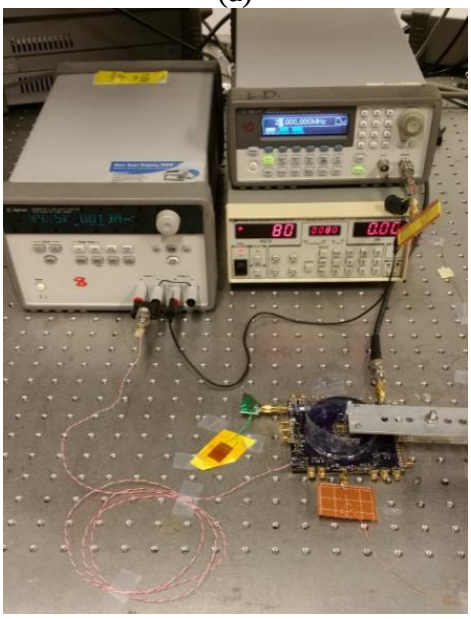
CMUTs in Rx mode is not negligible. Hence, M2 reduces the TIA input impedance for the inactive channels and significantly reduces the coupled voltage.

To reduce noise and interference in the following stages, a single-to-differential converter (STDC) is used (Fig. 5.9), consisting of a source follower, CS amplifier, and fully-differential amplifier with 22~49 MHz bandwidth and 6 dB gain. The positive/negative output balance is improved via source degenerated CS amplifier, while source follower acts as buffer and phase shifter. Following the STDC, a quadrature sampler extracts the envelope of the echo signal by converting it to baseband. The DLL generates 16 evenly delayed signals for an edge combiner to generate 40 MHz sine (I) and cosine (Q) waves. Two double-balanced mixers are used because of their low noise and high linearity. This approach reduces the bandwidth (and the size) requirement on the cable carrying the echo signals.

In the Tx mode, as shown in Fig. 5.1, M1 is opened (A=0 V), M2 is closed (D=1.8 -V), and M3 is closed (B=39 V) to charge the CMUT for 12.5ns. M3 is then opened (B=44 -V) and M4 is closed (C=5 V) for 300ns to reduce the effect of membrane ringing, then both of M3 (B=44 V) and M4 (C=0 V) are opened to force the CMUT output current flowing into the TIA input. The pulser consists of lateral double-diffused (LD) PMOS and NMOS, driven at 5V, while the control logic is supplied at 1.8V. To achieve sharp impulse with small LDMOS, level shifters convert 1.8V to 5V gate drive for LDNMOS (M4), while an additional CS amplifier with a diode-connected PMOS load is used to generate 39 V – 44 V gate drive for LDPMOS (M3). To make edges of the gate voltage sharper, an inverter chain follows the amplifier. When the Tx channel is deactivated, M4 is closed to prevent



(a)



(b)

Figure 5.11. (a)Microphotograph of guidewire ultrasound imaging SoC prototype, (b) measurement setup.

undesired firing from the parasitic coupling of the adjacent firing channels. The measured spectrum of Tx pressure pulses show 32-42MHz -3dB bandwidth.

5.2.2 Measurement results

A 16-ch GUISoC prototype was fabricated in the TowerJazz 0.18-µm HV-CMOS process, occupying 1.5 mm^2 of the active area (Fig. 5.11a). This size is readily suitable for

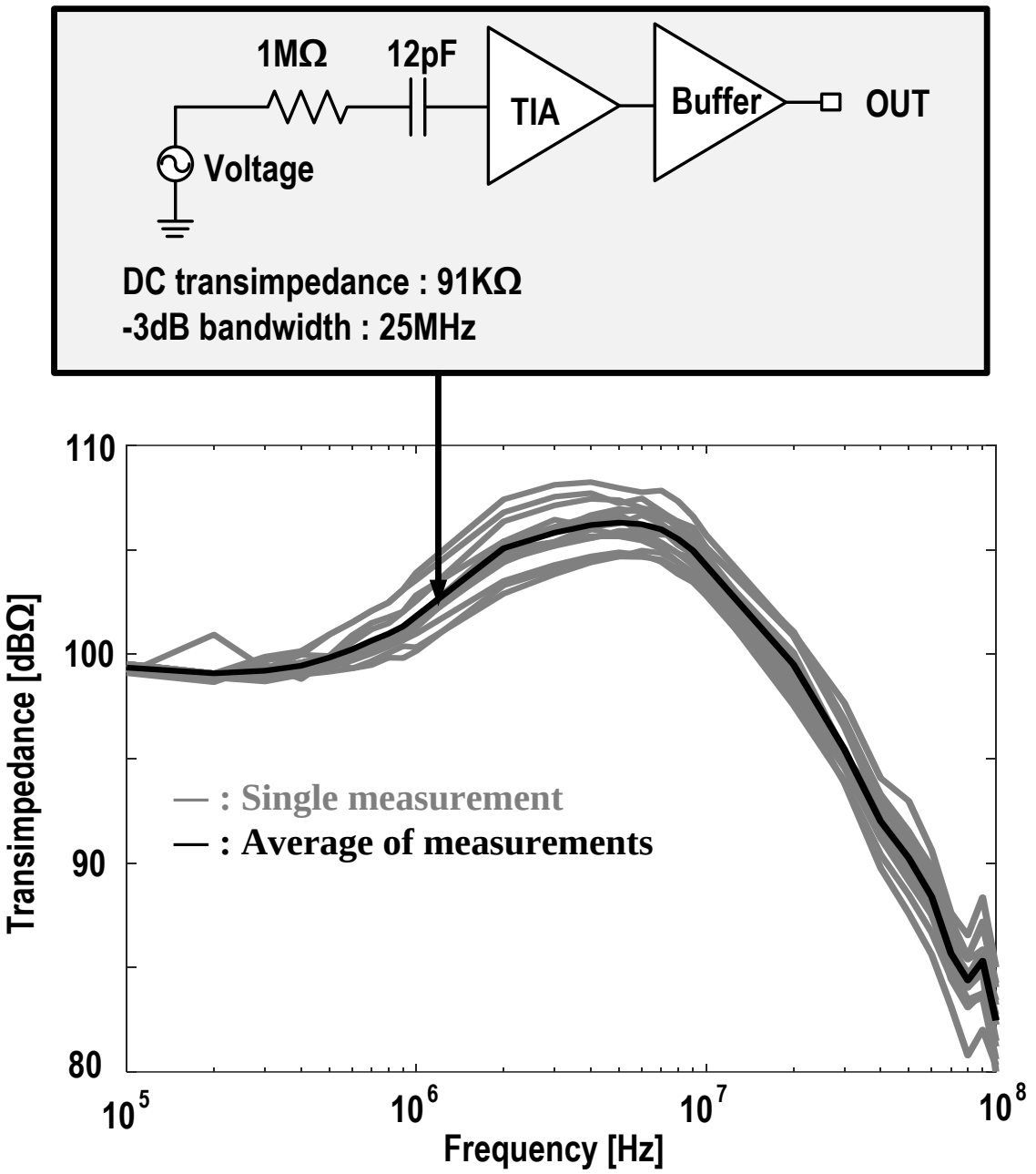


Figure 5.12. Measured transimpedance of the 12 TIAs in a chip.

integration on a 0.035" guidewire on a 0.7mm × 2.3mm footprint. In the experimental setup (Fig 5.11b), the output signal was received by a 250MHz digitizer (M3i.4142, Spectrum) through a 2m long 52AWG coaxial cable suitable for guidewires. The power consumption of the entire system at was 25.2mW plus 44mW from 1.8V and 44V supplies, respectively. A separate 80V was needed to bias the current CMUT prototype. External capacitors of

Table 5.1 – Performance summary and benchmarking of GUISoC

	[96]	[56]	This work
CMOS Technology	TSMC 0.35 µm	TSMC 0.18 µm HV	TowerJazz 0.18 µm HV
Active area (mm^2)	1.33	1.32	1.5
Power consumption	52.8@3.3V	14.3mW@1.8V 52.4mW@30V	25.2mW@1.8V 44mW@44V
Number of T/Rx channel	8(Rx only)	4	16
-3dB bandwidth of TIA(MHz)	20	5.2	25
Transimpedance of TIA	28.5 kΩ	67.6 kΩ	91 kΩ
-3dB bandwidth of TIA+CMUT(MHz)	33 - 42	-	30 - 38.5
Output referred noise of TIA (nV/√Hz)	28@40MHz	91@3MHz	47@40MHz
Conversion gain of mixer + gain of STDC	12 dB	-	6 dB
-3 dB bandwidth of mixer +STDC (MHz)	7	-	9.5
RMS of clock jitter (ps)	114	-	215
Transmitter output pressure bandwidth (MHz)	-	-	32 - 42

1uF, 1nF, 200 pF were added to the 1.8V regulator, HV regulator, respectively, when operating the system. These capacitors are small enough to be embedded underneath the CMUT-on-CMOS, as shown in Fig. 5.8.

The TIA measurement results showed average 91 kΩ transimpedance, 47 nV/√Hz output-referred noise, and 25 MHz bandwidth (Fig. 5.12). When The pressure to voltage bandwidth was reduced to 25-38 MHz when TIA was measured together with a CMUT. The clock multiplier showed 215ps RMS jitter when generating 40 MHz square waves.

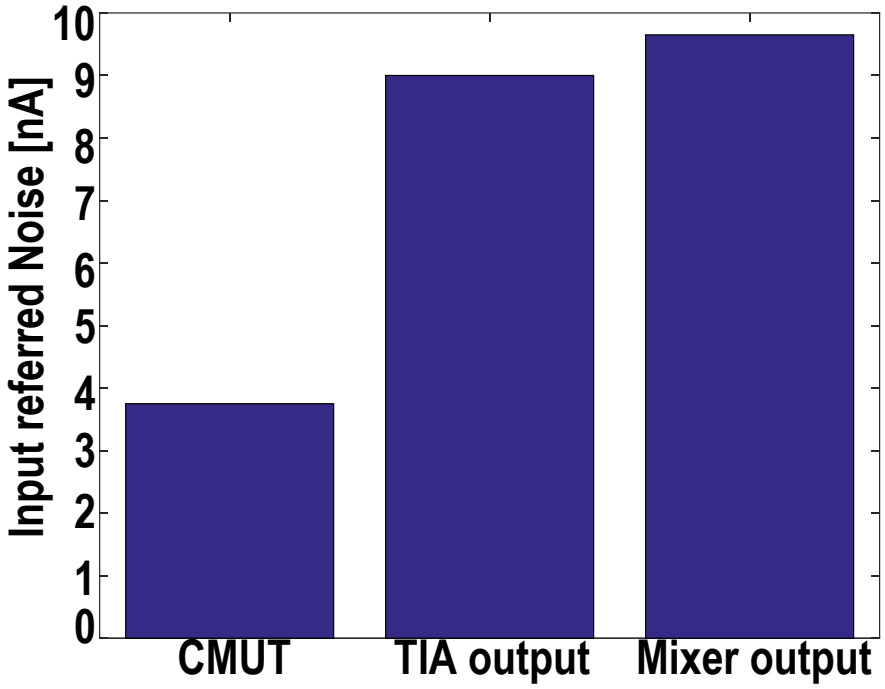


Figure 5.13. Measured input-referred noise from CMUT, TIA output, and Mixer output.

Measured PSRR of the HV regulator was -60dB at 20MHz with 1nF load capacitor. Table 5.1 summarizes the GUISoC specifications.

Fig. 5.13 shows measured input-referred noise of the system from the important outputs. CMUT itself generates 3.75 nA, and TIA output shows 9 nA in the bandwidth of 35 – 45 MHz. Although we designed the TIA noise to be a similar level of CMUT noise, the switch (M1 in Fig. 5.8) added twice more noise than that of TIA, which is unpredictable in the simulation. Therefore, the entire noise from CMUT to TIA output become 9 nA. The mixer and S-to-D converter added 3.5 nA as an input-referred noise.

We conducted successful real-time imaging tests with the GUISoC and a 12-element CMUT array prototype. For this experiment, the GUISoC and interconnects were coated with 1-μm thick Parylene above the entire PCB and epoxy on the boundaries for electrical isolation. The measured spectrum of Tx pressure pulses show 32 – 42 MHz

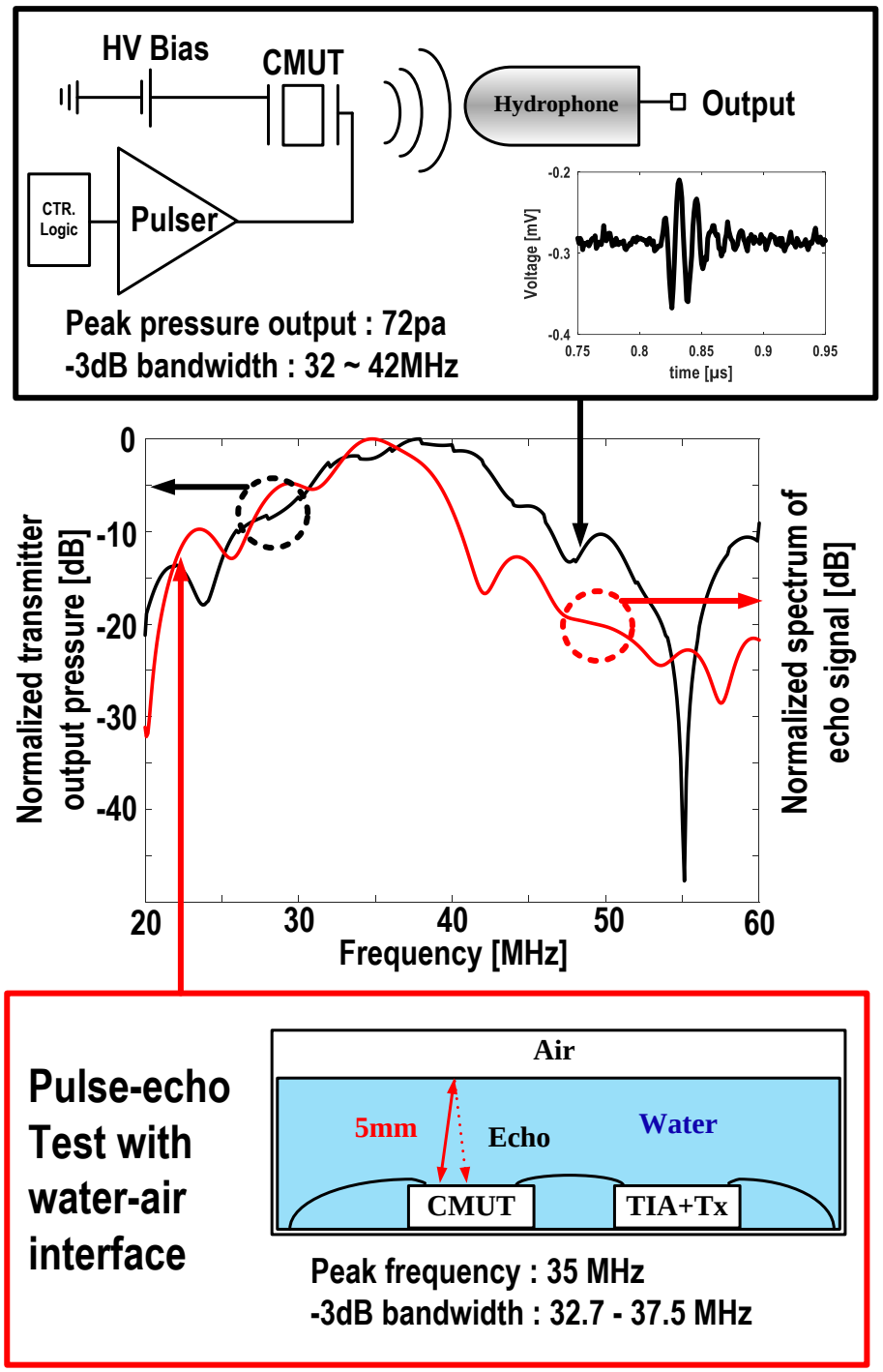


Figure 5.14. Measured spectrum of CMUT+pulser output pressure and pulse-echo from the water-air interface.

-3 dB bandwidth (Fig. 5.14). The imaging target was three 100 μm dia. wires immersed in water, similar to coronary stent struts. The average of measure SNR from the first wire target was 18 dB. Fig. 5.15 shows the constructed image, in which wires are clearly

distinguishable. The lateral resolution of 3rd the wire at 7 mm distance was 560 μm, in agreement for a 300 μm aperture at 37 MHz.

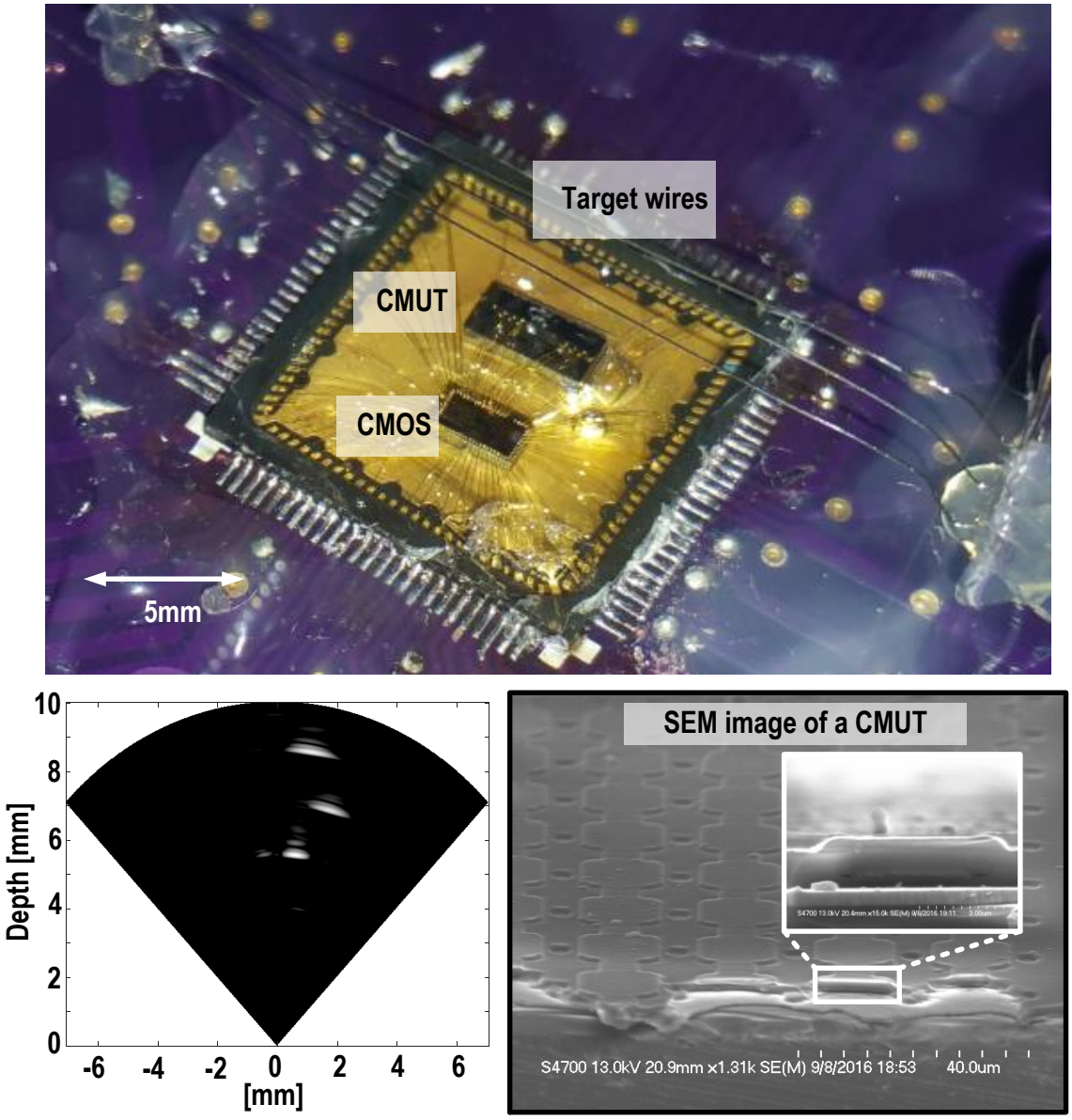


Figure 5.15. Measurement setup consisting of three 100μm diameter wires above the CMUT array immersed in water (top) and reconstructed image (bottom).

5.3 Wireless read-out SoC for high-frequency ultrasound imaging

Similar to the wireless read-out system described in Chapter. 4, we can adopt IR-PWM to reduce one more wire.

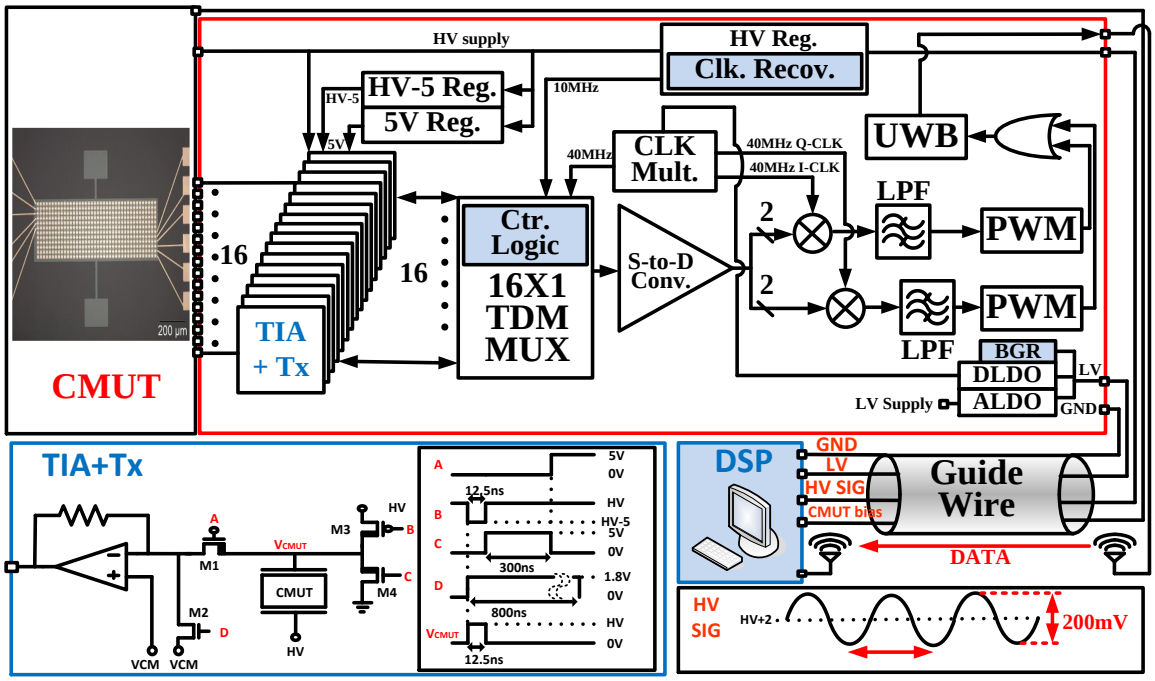


Figure 5.16. Overall system block diagram of the proposed wireless read-out SoC for high frequency ultrasound imaging.

5.3.1 Wireless read-out SoC for high-frequency ultrasound imaging

Until the low-pass filters (LPF) in Fig. 5.16 (part of quadrature sampler), the system shares basic structure with the system described in section 5.2. After, the quadrature sampler, we adopted the impulse-radio pulse width modulator (IR-PWM) (described in chapter 3), which reduce one more wire for the data output. In this chip, we did some minor revision from previous systems. First of all, we increased HV supply up to 55 V to give larger pulse, generating more electrical force on CMUT membrane. The PMIC, described in Fig. 5.10, requires to apply a sinusoidal wave with 3 $V_{p\text{-}p}$ amplitude because of two problems: improper impedance matching at HV SIG and difference of DC voltage between

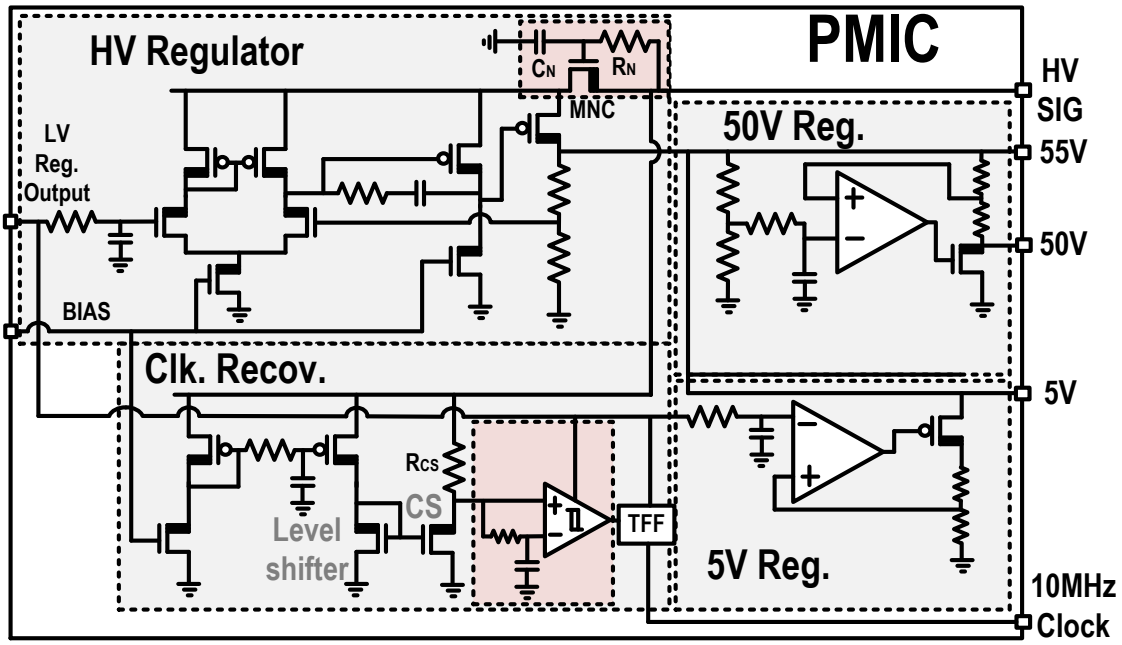


Figure 5.17. Block diagram of the modified PMIC.

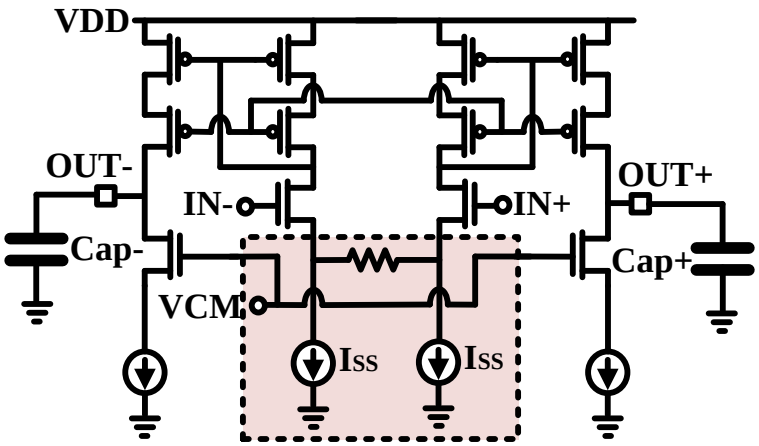


Figure 5.18. Block diagram of the modified OTA for IR-PWM.

CS amplifier output in Fig. 10 and threshold of the following inverter. Since the coaxial cable which delivers HV SIG is matched to 50 Ω, it is better to make input impedance of HV SIG 50 Ω to prevent reflection from the circuit. Thus, we changed R_N to 50 Ω, and increase the capacitance of C_N to be 1 nF to suppress 20 MHz sinusoidal wave. On the other hand, we also changed clock recovery part. the system in section 5.2 used an inverter

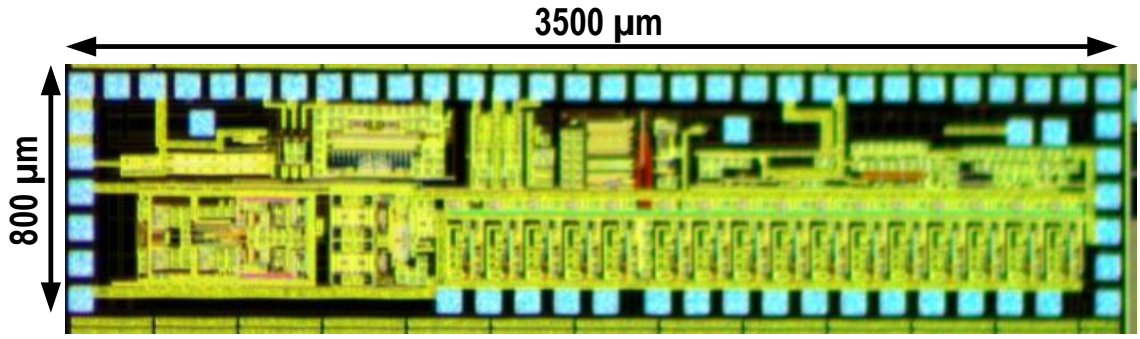


Figure 5.19 Die photomicrograph of the wireless read-out SoC for high frequency ultrasound imaging**.**

as a single input comparator and modified the R_{CS} to make DC level of the CS output become similar to switching voltage of the inverter. However, the DC voltage varies with the resistance of R_{CS} and bias current, which have large chip-to-chip variation in the given process (TowerJazz 0.18-µm HV CMOS). To make the system robust, we used a comparator instead of the inverter, and, by using an RC low-pass filter at one of the input, we recover the clock regardless of R_{CS}.

Aside from PMIC part, we also modified the OTA used (Fig. 5.18) in IR-PWM. In Fig. 3.5a, we used two separate resistors as source degeneration resistor for each input of the differential input pair. That not only increases area but also decreases the headroom at the lower limit of input. If we place the degeneration resistor between the source of input pairs, we still achieve the high linearity addressing the problems stated above. To decrease clock jitter on the clock for the PWM, we implemented one more LDO only for the clock multiplier.

5.3.2 Measurement results

The proposed wireless read-out SoC for high-frequency ultrasound imaging was fabricated in the TowerJazz 0.18-µm HV-CMOS process, occupying 1.98 m^2 of the active

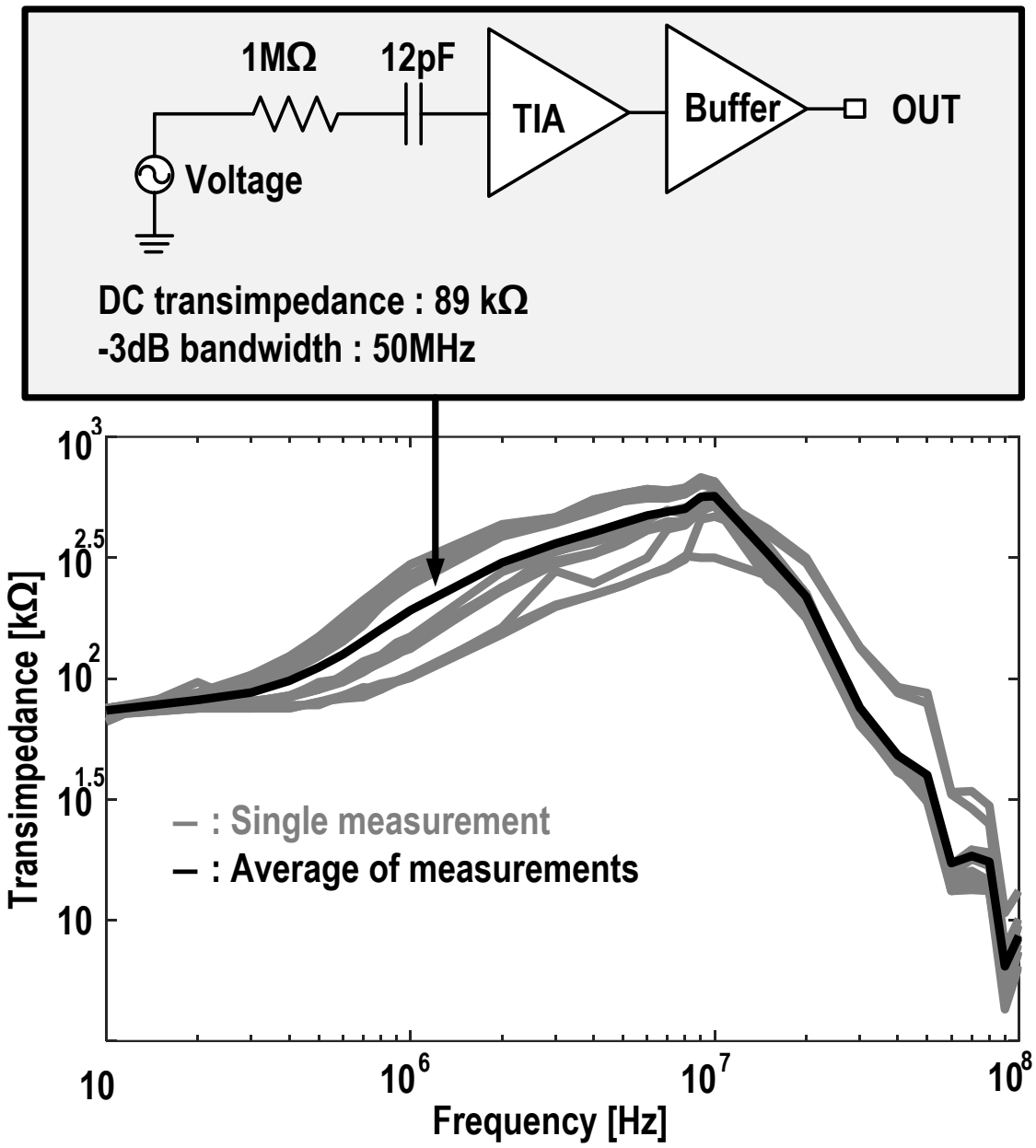


Figure 5.20 TIA measurement results of 16 TIAs.

area (Fig. 5.19). The power consumption of the entire system at was 28.5 mW plus 84 mW from 1.9 V and 56 V supplies, respectively. Since we used the same process as the system in section 5.2, most of the parts show almost same results of the system in section 5.2. The TIA measurement results showed average 89 kΩ transimpedance, and 50 MHz bandwidth (Fig. 5.20). The mixer and S-to-D converter shows 6 dB gain with -3dB bandwidth of

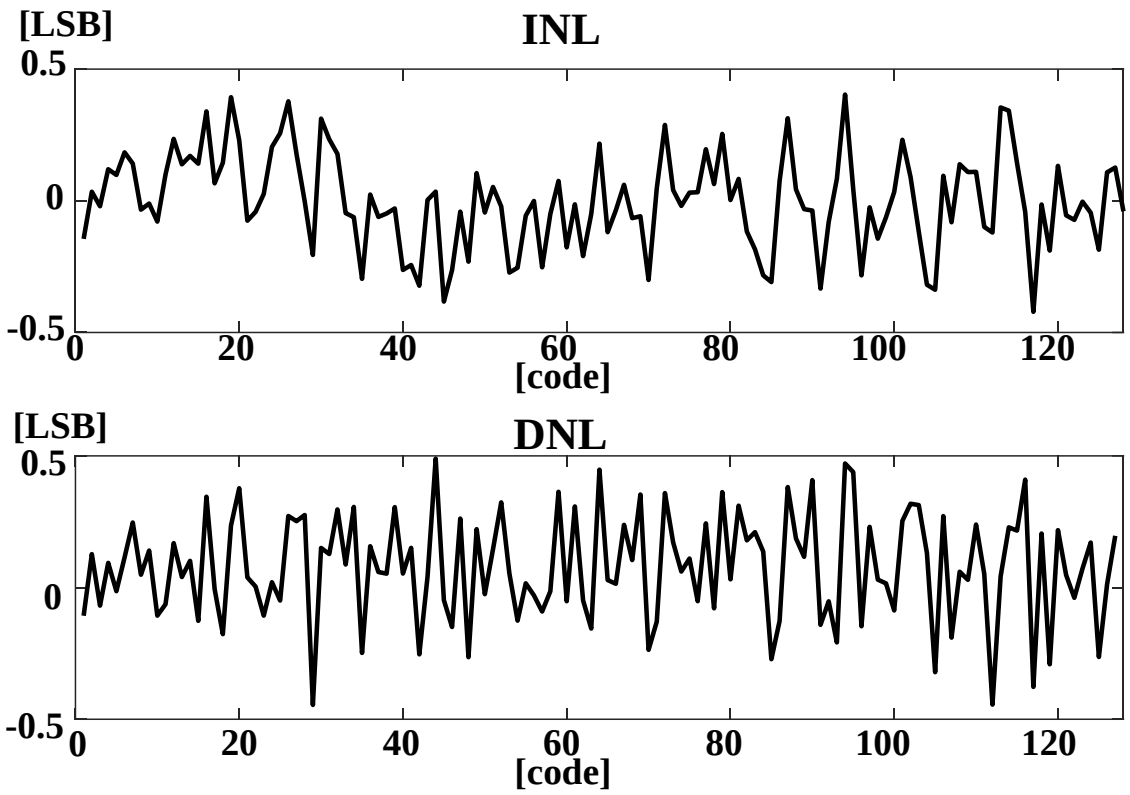


Figure 5.21 Measured INL (top) and DNL (bottom) of IR-PWM.

9.5 MHz. Although we changed OTA little bit, we still got 7-bit resolution (Fig. 5.21). We applied 0.2-$V_{peak\text{-}to\text{-}peak}$ 20MHz sinusoidal wave on top of 56 V DC at HV SIG, and we got 55 V DC and 10 MHz clock from the HV regulator. We used two 1nF capacitors as load capacitor of the HV LDO and C_N in Fig. 5.17.

Since we ran out of CMUTs, we applied emulated signal as an input signal. In Fig. 5.22, we showed reconstructed I/Q signals. To show the functionality of the SoC, we showed the outputs of the SoC were well matched with the down converted I/Q signal from the input signal, calculated in MATLAB (Fig. 5.22). The measured IR-PWM signal shows 135 ps RMS noise which represents 2.7 mV_{rms} as an input-referred noise of IR-PWM. The measured maximum peak signal from I or Q was 0.23 V, which resulted in 38.6 dB SNR.

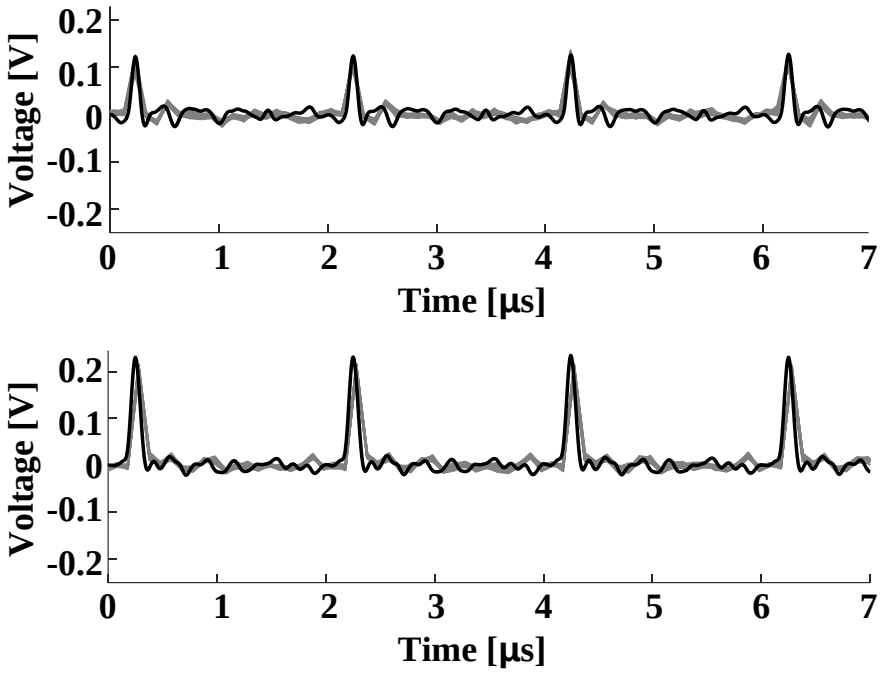


Figure 5.22 Reconstructed IR-PWM output from the SoC.

CHAPTER 6. CONCLUSION AND FUTURE WORK

This dissertation focuses on developing innovative circuit and systems for intravascular or wireless ultrasound imaging system, which results in several publications [59], [96], [106]-[109]. The proposed intravascular ultrasound imaging (IVUS) system reduced a required number of interconnection, that is important to integrate the system on a guidewire (nominal diameter of 0.35-0.9 mm), by implementing on-chip bias, power management, and digital control logic circuits. In addition, since the thickness of the wire is also important. The thinner is preferable for the system to be more flexible, while high-frequency signal requires a thicker wire to secure wide bandwidth which can cover echo signal bandwidth. Consequently, we adopted on-chip clock multiplier and down conversion mixer to reduce the signal bandwidth narrower by down-converting RF signal (echo signal) to base band.

6.1 Conclusion of reduced-wire guidewire IVUS system

The prototype of 16-ch reduced-wire guidewire IVUS was fabricated and tested in the TowerJazz 0.18-μm HV-CMOS process, occupying 1.5 mm^2 of the active area (Fig. 5.10). This system can be integrated on a 0.035" guidewire on a 0.7mm × 2.3mm by adjust the footprint and remove unnecessary test blocks. The prototype successfully constructed images with a 250MHz digitizer (M3i.4142, Spectrum) through a 2 m long 52 AWG coaxial cable suitable for guidewires. The power consumption of the system at was 25.2mW and 44mW from 1.8V and 44V supplies, respectively. Although a separate 80V was needed to bias the current CMUT prototype, it can be shared with the same 44V (HV) that supplies the Tx block when the target CMUT is successfully fabricated. Now, the

capacitors of 1uF, 1nF, 200 pF, which are required for the 1.8V regulator, HV regulator, respectively, as an external capacitor. However, the capacitors are small enough to be fabricated below the CMUT-on-CMOS. The system works with the TIA with average transimpedance of 91 kΩ, 47 nV/√Hz output-referred noise, and 25 MHz bandwidth. The pressure to voltage bandwidth, which measured with a CMUT array in [104], was 25-38 MHz. The clock multiplier showed 215ps RMS jitter with 40 MHz square wave, and measured PSRR of the HV regulator was -60dB at 20MHz with 1nF load capacitor.

The ASIC and interconnects were coated with epoxy first and 5-μm thick Parylene was coated above the entire PCB to electrically isolate the system from the water, which used as the medium, for imaging test. The experiment successfully imaged the three-wire target (Fig 5.13), and the lateral resolution of 3rd the wire at 7mm distance was 560μm, in agreement for a 300μm aperture at 37MHz. The key specification and comparison with recent papers are summarized in Table 6.1.

Table 6.1 – Key specification and benchmarking table

	[67]	[56]	This work
CMOS Technology	TSMC 0.35 µm	TSMC 0.18 µm HV	TowerJazz 0.18 µm HV
Active area (mm^2)	6.16	1.32	1.5
Power consumption	20mW@3.3V -@25V*	14.3mW@1.8V 52.4mW@30V	25.2mW@1.8V 44mW@44V
Number of T/Rx channel	56/48	4/4	16/16
-3dB bandwidth of TIA(MHz)	40	5.2	25
Transimpedance of TIA	200 kΩ	67.6 kΩ	91 kΩ
-3dB bandwidth of TIA+CMUT(MHz)	-	-	30 - 38.5
Output referred noise of TIA (nV/√Hz)	62@20MHz	91@3MHz	47@40MHz
Number of connections	13	-	4
Wireless coommunication	No	No	Yes

*Power consumption at Tx was not mentioned in the paper.

6.2 Future work of the reduced-wire guidewire IVUS system

To fit the proposed IVUS system on a 0.35-mm guidewire, we concluded that it is better to remove the direct down-conversion part (mixer, clock multiplier, and S-to-D converter), and use wider band coaxial cable for the RF output (echo signal). Since the CMUT array is vulnerable to parasitic, minimizing the parasitic by putting CMUT and CMOS close each other is required. As we proposed in [67], the CMUT-on-CMOS is the most promising way to closely implement CMUT and CMOS. For that purpose, we designed and fabricated the ASIC for CMUT-on-CMOS (Fig. 6.1). The ASIC consists of 16-ch TRX for CMUT array (TIA+ pulser), regulators for high voltage (HV) supplies, an on-chip bias generator, and wideband buffer (more than 50 MHz bandwidth). The system

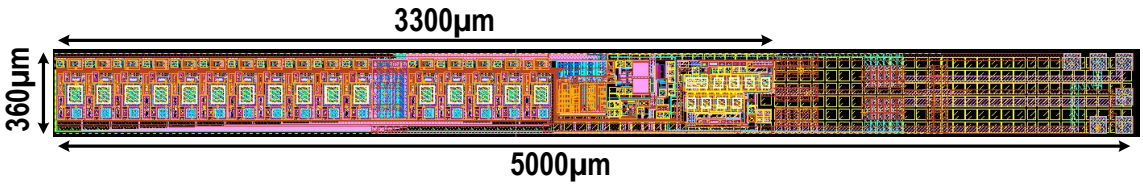


Figure 6.1. Layout of the ASIC for CMUT-on-CMOS.

requires six connections: RF output, low voltage (LV) supply, HV supply, ground, Clock, and CMUT bias. As mentioned previously, the CMUT bias and HV supply will be connected each other with the targeted CMUT array.

6.3 Conclusion of wireless ultrasound imaging system

We have presented a proof-of-concept prototype of a wireless read-out interface SoC for guidewire IVUS imaging system. It includes a quadrature sampler and the IR-PWM for the high-frequency ultrasound imaging with only four connections: HV SIG, LV, GND, and CMUT bias (in Fig. 5.16). The CMUT bias can be exported from HV SIG if the CMUT become compatible with HV supply on the SoC. Despite, because lack of the CMUT, we could not show imaging capability, we showed functionality of the SoC with emulated input signal from the ASIC fabricated in TowerJazz 0.18-µm HV CMOS process.

6.4 Future work of wireless ultrasound imaging system

So far, we use log periodic antenna, which is too large to implement inside of the body. Therefore, compact size wideband antenna should be designed to implement. As a candidate of the compact size antenna, we conducted preliminary research about mono pole antenna with a single wire.

Since the acoustic reflection at the blood-tissue interface is about -40 dB, the imaging system should have at least 50 dB of dynamic range [99]. If the readout system

has a 7-bit resolution, it can only provide a dynamic range of 40 dB for single-pulse echo signal. However, synthetic aperture imaging with N firings provides an additional 10log(N) dB improvement in the overall SNR compared to a single-pulse and single channel [110]. Considering the width of the CMUT array (300 μm) and the width of each element, $\lambda/2 \approx$ 15 μm at 40 MHz, it is possible to have 120 independent firings to improve the overall SNR by about 20 dB over a single channel to achieve 60 dB dynamic range in the resulting image. Moreover, even though the 6-bit resolution of the ATC in the current prototype SoC is lower than the 7-bit design target, it is possible to improve this figure by reducing the noise on the reference nodes by the more careful layout and additional capacitors or buffers. Migrating the SoC to a CMOS process with smaller feature size will reduce the setup and hold times of the flip-flop used in the DLL as a PFD, and increase the speed of the edge combiner, while reducing the clock jitter.

Current ASIC is built in a single layer CMOS chip. However, by using multi-layer chips connected by through-silicon via (TSV), we could save more area. The SoC can be easily divided into three separate compartments: 1) PMIC, 2) analog front end (AFE), and 3) control logic + RF blocks. Four CMUT arrays are going to be integrated on the guidewire IVUS to cover the entire cross-section of the artery, limiting the size of each chip to about 300 μm × 1 mm. Even though each CMUT array needs its own AFE, all four AFEs can share the same PMIC, control logic, and RF blocks. Therefore, by thinning and stacking these compartments, using the 3D-IC technology [111] which employs TSV for interconnects among three compartments, it is possible to shrink the interface SoC to the desired size for guidewire IVUS application.

The large and low-frequency antennas used in the current prototype experimental setup can be replaced with either dipole or on-chip antennas in the next revision of the SoC, which will be implemented in a smaller feature size process with faster transistors that can generate sharper and narrower impulses within 3~5 GHz band. Several mm-sized on-chip antennas for IR-UWB based short-range communication have already been reported in the literature [112], [113]. In the IVUS application, IR-Tx antenna will be inside of the body. The length of the dipole antenna is proportional to $1/\sqrt{\varepsilon_r}$, where ε_r is the relative permittivity of the transmission medium. In the tissue, $\varepsilon_r \approx 50$ in 3-5 GHz band [114]. Therefore, the optimal length of the dipole antenna will be 7 times shorter than a similar antenna in air. Since our target communication distance is quite short, from inside the heart to the surface of the chest, even a non-ideal antenna could be sufficient. The path loss across a 5 cm distance in the human torso in this frequency range is about 40 dB [115]. Therefore, the required IR-Tx output power, in this case, can be calculated from,

$$P_{TX} = SNR + Path\,loss + N + 10\log_{10}(BW) + NF + I, \tag{7.1}$$

where *N* is the IR-Rx noise floor, BW is the channel bandwidth, NF is the noise figure, and I is the implementation loss, which has a nominal value of 1 dB [116]. A generic commercial UWB receiver [117], has NF = 7 dB and N = -174 dBm/Hz at room temperature. In terms of the required SNR, if we do not consider inter-symbol interference, the PWM-IR-UWB can be analyzed similarly to on-off keying (OOK). If we set the maximum required bit-error-rate (BER) to 10^{-3}, which can be further improved using digital signal processing, the required energy per bit over noise power spectral density

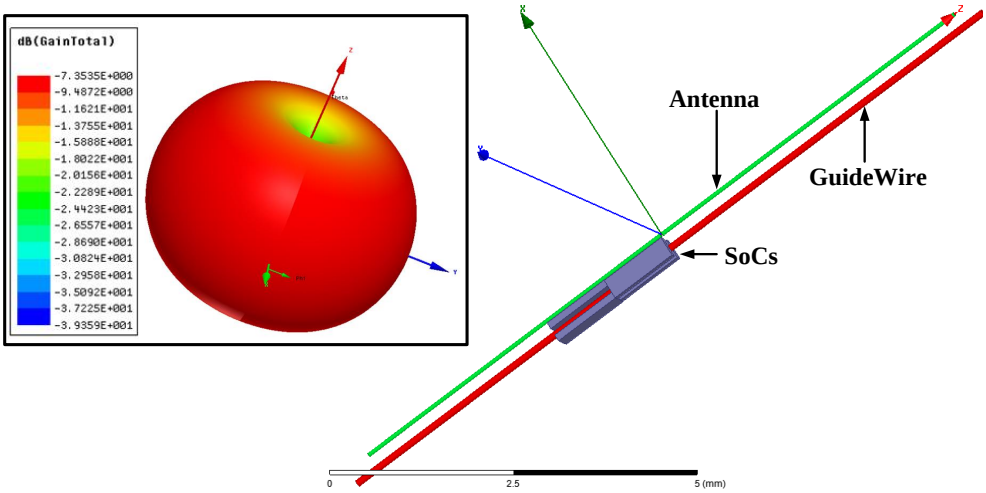


Figure 6.2. (a) Dipole antenna simulation model in the HFSS environment, extending from the interface SoC at the tip of the guidewire IVUS; inset: Simulated antenna gain and its omnidirectional characteristic.

(E_b/N_0) would be 9 dB [118]. The time resolution of the ATC block with 7-bit resolution and 20 MS/s is 390 ps. Therefore, the PWM equivalent data rate with OOK modulation would be 2.5 Gb/s. Now we can use,

$$SNR = 10\log_{10}\left(\frac{E_b}{N_0}\cdot\frac{DR}{BW}\right), \tag{7.2}$$

where DR is the data rate [118], to calculate the required SNR for the PWM, which is 10.7 dB. In this case, the required IR-Tx output power would be -22.3 dBm. Fig. 6.2 shows the HFSS simulation of a dipole antenna in the tissue environment that extends from both sides of the interface SoC at the tip of the guidewire IVUS. Minimum gain of this antenna in the valid range of 20° < theta < 160° is -18 dB. On the IR-Rx side, the external antenna can be a commercial patch or log-periodic antenna with the gain of 6 dBi [119]. Therefore, the required IR-Tx output power would be -10.05 dBm, which is well within the power budget for this block. These calculations show that a two-wire guidewire IVUS imaging system with IR-UWB wireless data link is feasible.

Similar to section 6.2, we also designed a wireless readout system ASIC for CMUT-on-CMOS fabrication (Fig. 6.3). This system requires three connections: LV supply, the clock on top of HV DC voltage, and ground. The CMUT bias will be provided by HV DC voltage that is regulated by an on-chip HV regulator. Since its width is 710 µm, it cannot be integrated 0.35-mm guidewire. However, considering 0.89-mm guidewire, it is a viable option.

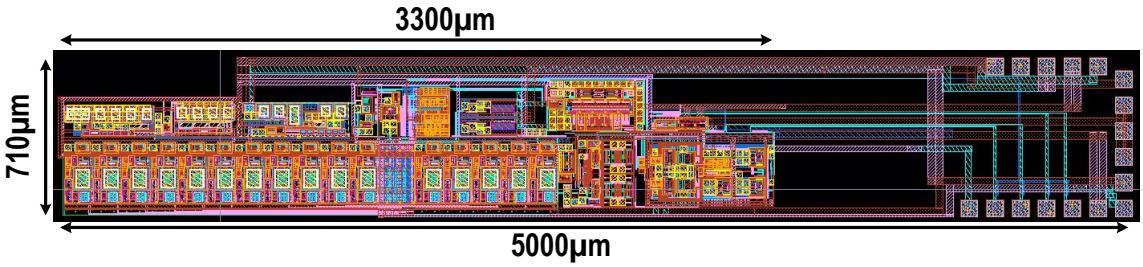


Figure 7.3. Layout of CMUT-on-CMOS for wireless ultrasound imaging system.

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